

Compal Confidential

Model Name : B4DBU(WIFI) / B4DBG(LTE)
File Name : LA-D301P
BOM P/N:43

Compal Confidential

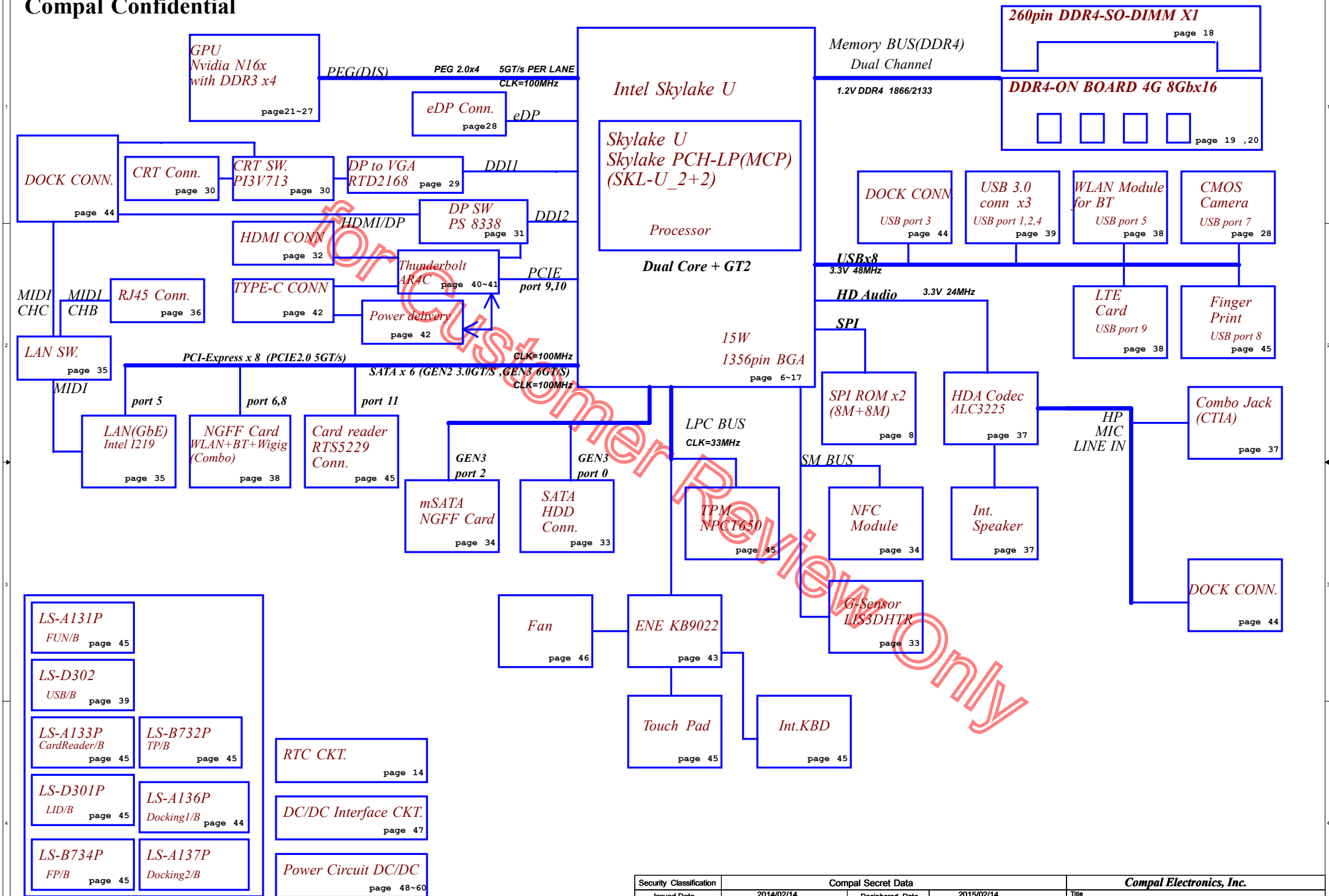
B4DBU(WIFI) / B4DBG(LTE)
M/B Schematics Document

Skylake U Processor + DDR4 + Nvidia N16X

2015-12-09

Rev:1.0

Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date		2014/02/14	Deciphered Date	2015/02/14	Title
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		LA-D301P			0.1
		Date: Thursday, December 17, 2015			Sheet 1 of 63



Vcc	3.3V +/- 5%				
Ra	100K +/- 5%				
Board ID	Rb	V_{BI}D min	V_{BI}D typ	V_{BI}D max	EC AD3
0	0	0 V	0 V	0.300 V	0x00 - 0x0B
1	12K +/- 1%	0.347 V	0.345 V	0.360 V	0x0C - 0x1C
2	15K +/- 1%	0.423 V	0.430 V	0.438 V	0x1D - 0x26
3	20K +/- 1%	0.541 V	0.550 V	0.559 V	0x27 - 0x30
4	27K +/- 1%	0.691 V	0.702 V	0.713 V	0x31 - 0x3B
5	33K +/- 1%	0.807 V	0.819 V	0.831 V	0x3C - 0x46
6	43K +/- 1%	0.978 V	0.992 V	1.006 V	0x47 - 0x54
7	56K +/- 1%	1.169 V	1.185 V	1.200 V	0x55 - 0x64

BOM Option Table		BOM Option Table		
Item	BOM Structure	Item	BOM Structure	
Unpop	@	dGPU	VGA@	
Connector	CONN@	SAMSUNG DDR4	X76SAM@	
EMC requirement	EMC@	N16S-GT	SGT@	
EMC requirement depop	@EMC@	Without WiGi Funct i on	NOWG@	
EMI requirement	@EMC@/EMI@	HDD Redriver	X76TI@/X76PAR@	
Thunderbolt Funct i on	TBT@	GPU CG6 funct i on	VGM@	
RF requirement	@RF@/RF@	VRAM BOM Select	X76@	
LTE Funct i on	3G@	Single/Dual Rank	SR@/DR@	
UMA only	UMA@		DR@ is not been used in this project)	
VPRO Funct i on	VPRO@/NOVPRO@		PD Funct i on	PD@
VGA EMI Requirement	@VGA_EMI@/VGA_EMI@		CPU Code	QH7Y@
VGA UNPOP	@VGA@	CPU Code	QH7Y@	
VGA RF Requirement	@RF@_VGA@			
VGA Power	22@/23E@			
GC6 Funct i on	GC6@/NGCG6@/NGC6			
INTEL CMC	CMC@			
ESPI	ESPI @			

BUS	Device	Address(7 bit)	Address(8bit)	
			Write	Read
I2C_0 (+3VS)	Reserved (Touch Panel)			
I2C_1 (+3VS)	TM-P2969-001 (TP)	0x2C		
	SB8787-1200 (TP-ELAN)	0x16		
SOC_SMBCLK +3VS	DIMM1	0xA0		
	DIMM2	0xA4		
	LIS3DHTR(G-Sensor)	0x30		
SOC_SML1CLK +3VS	N16S-GT (VGA)	0x9E		
	PCH-LP (SOC)	0x90		
EC_SMB_CK1 +3VLP	BQ24780 (Charger IC)	0x12		
	BATTERY PACK	0x16		
SOC_SML0CLK +3VS	LAN	0xC8		
	NFC	0x28		

43 Level	Description	BOM Structure
431A0NBOL01	SMT MB AD301 B4DBG QJFC 2.3G UMA HDMI	3G@/CMC@/DA2@/SR@/EMC@/EMI@/ESD@/HDMI@/NOVPRO@/PD@/TBT@/UMA@/X76PAR@/X76SAM@/RF@
431A0NBOL02	SMT MB AD301 B4DBG QJ8M 2.4G UMA HDMI	3G@/CMC@/DA2@/SR@/EMC@/EMI@/ESD@/HDMI@/NOVPRO@/PD@/TBT@/UMA@/X76PAR@/X76SAM@/RF@
431A0NBOL03	SMT MB AD301 B4DBG QJKP 2.3G DIS HDMI	3G@/CMC@/DA2@/SR@/EMC@/EMI@/ESD@/GC6@/HDMI@/PD@/SGT@/TBT@/VGA@/VGA_EMI@/VPRO@/X76PAR@/X76SAM@/RF@
431A0NBOL04	SMT MB AD301 B4DBG QJJK 2.5G DIS HDMI	3G@/CMC@/DA2@/SR@/EMC@/EMI@/ESD@/GC6@/HDMI@/PD@/SGT@/TBT@/VGA@/VGA_EMI@/VPRO@/X76PAR@/X76SAM@/RF@

STATE \ SIGNAL	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
S0 (Full ON)	HIGH	HIGH	HIGH	ON	ON	ON	ON
S3 (Suspend to RAM)	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)	LOW	LOW	LOW	ON	OFF	OFF	OFF

Power Plane	Description	S0	S3	S4/S5
+19V_VIN	Adapter power supply	N/A	N/A	N/A
+17.4V_BATT	Battery power supply	N/A	N/A	N/A
+19VB	AC or battery power rail for power circuit.	N/A	N/A	N/A
+VCC_CORE	Processor IA Cores Power Rail	ON	OFF	OFF
+VCC_GT	Processor Graphics Power Rails	ON	OFF	OFF
+VCC_SA	System Agent power rail	ON	OFF	OFF
+0.6VS_VTT	DDR +0.6VS power rail for DDR terminator .	ON	OFF	OFF
+1.0VALW_PRIM	+1.0V Always power rail	ON	ON	ON*1
+1.0V_VCCSTU	Sustain voltage for processor in Standby modes	ON	ON	OFF
+VCCIO	CPU IO power rail	ON	OFF	OFF
+1.0VS_VCCSTG	+1.0VALW_PRIM Gated version of VCCST	ON	OFF	OFF
+1.2V_VDDQ	DDR4 +1.2V Power Rail	ON	ON	OFF
+1.8VALW_PRIM	+1.8V Always power rail	ON	ON	ON*1
+1.8VS	System +1.8V power rail	ON	OFF	OFF
+3VLP	+19VB to +3VLP power rail for suspend power	ON	ON	ON
+3VALW	System +3VALW always on power rail	ON	ON	ON*1
+3VS	System +3V power rail	ON	OFF	OFF
+5VALW	+5V Always power rail	ON	ON	ON
+5VS	System +5V power rail	ON	OFF	OFF
+RTCVCC	RTC Battery Power	ON	ON	ON
+1.05VSDGPU	+1.05VS power rail for GPU	ON	OFF	OFF
+1.5VSDGPU	+1.5VS power rail for GPU	ON	OFF	OFF
+3VSDGPU_AON	+3VS power rail for GPU(AON rails)	ON	OFF	OFF
+3VSDGPU_MAIN	+3VS power rail for GPU GC62.0	ON	OFF	OFF
+VGA_CORE	Core power for discrete GPU	ON	OFF	OFF
+2.5V	DDR4 +2.5V Power Rail	ON	ON	OFF

Note : ON*1 means power plane is ON only when WOL enable and RTC wake at BIOS setting, otherwise it is OFF.

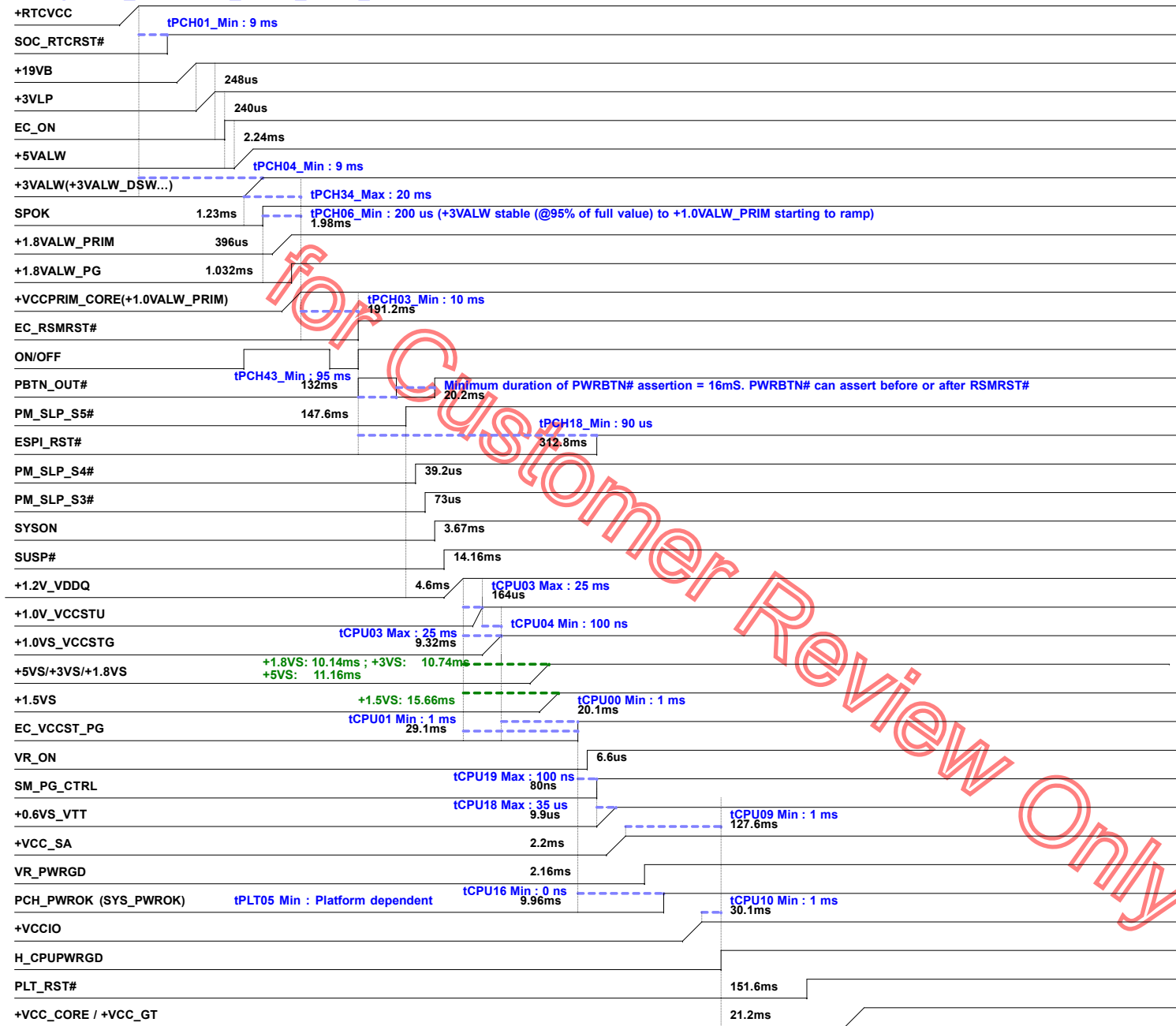
Board ID	PCB Revision
0	0.1
1	0.2
2	0.3
3	1.0
4	
5	
6	
7	

B4DBU64DBG LA-D301PR01_0630.DSN					
VR/Load SW	Power Rail Name	VR/Load SW	Power Rail Name	VR/Load SW	Power Rail Name
+19VB	PU9001 EN.DRVON	→ +VCC_CORE			
	PU9003 EN.DRVON	→ +VCC_GT			
	PU9004 EN.DRVON	→ +VCC_SA			
	PU501 EN.SYSON	→ +0.6VS_VTT			
		→ +1.2V_VDDQ	→ JPC1_JPC2 JUMP	→ +1.2V_VDDQ_CPU	→ RC208 0_ohm_0402 → +1.2V_VDDQC
+19VB				→ RC141 0_ohm_0402	→ +1.2V_VCCSFR_OC
	PU402 EN.SV_EN	→ +5VALW	→ U33 EN.USB_PWR_EN#	→ +USB3_VCCA	
			→ U5007 P365882	→ +5VALW_PD	
			→ U5008 EN.SUSP#	→ +5VS	→ U68 EN.+5VS → +VCC_FAN1
				→ U53 AP2330W-7	→ +HDMI_5V_OUT
+19VB				→ Q23_Q24 EN.KB_BL_EN	→ +5VS_BL
				→ RC229 0ohm_0603	→ +VDDA
				→ J2 Jump	→ +5VS_HDD
				→ R662 0ohm_0603	→ +5V_BST_NFC
+19VB	PU601 EN.+1.8VALW_PG	→ +1.0VALW_PRIM	→ UC5 EN.SYSON	→ +1.0V_VCCSTU	→ RC140 0ohm_0402 → +1.0V_VCCST
					→ RC143 0ohm_0402 → +1.0V_VCCSFR
			→ JPC9 JUMP	→ +1.0VALW_MPHYPLL	→ RC1409 0ohm_0603 → +1.0VALW_AMPHYPLL
				→ RC158 0ohm_0402	→ +1.0VALW_AP1LEB8
				→ RC209 0ohm_0603	→ +1.0VALW_MPHYGT
+19VB				→ RC178 0ohm_0603	→ +1.0VALW_SRAM
			→ RC162 0ohm_0402	→ +1.0VALW_DTS	
			→ RC192 0ohm_0603	→ +1.0V_PRIM_CORE	
			→ RC12 0ohm_0603	→ +1.0V_XDP	
			→ RC148 0ohm_0603	→ +1.0VALW_APLL	
+19VB			→ RC190 0ohm_0603	→ +1.0VALW_CLK4_F1000C	
			→ RC164 0ohm_0603	→ +1.0VALW_VCCCLK2	
			→ RC152 0ohm_0603	→ +1.0VALW_CLK5_F24NS	
			→ RC175 0ohm_0402	→ +1.0VALW_MPHYAON	
			→ RC169 0ohm_0402	→ +1.0VALW_CLK6_24TBT	
+19VB	PU1201 EN.DGPU_PWR_EN	→ +VGA_CORE			
	PU1001 EN.1.5VS_DGPU_P	→ +1.5VSDGPU			

+19VB	PU401 EN.SV_EN	→ +3VALW	→ JPC7 JUMP	→ +3VALW_PRIM	→ RC171 0ohm_0402 → +3VALW_RTC
					→ RC198 0ohm_0402 → +3VALW_HDA
					→ RC197 0ohm_0402 → +3VALW_1.8VALW_PGPPA
					→ RC161 0ohm_0402 → +3VALW_PGPPB
					→ RC163 0ohm_0402 → +3VALW_PGPPC
+19VB					→ RC172 0ohm_0402 → +3VAPW_-1.8VALW_PGPPD
					→ RC167 0ohm_0402 → +3VALW_PGPPF
					→ RC187 0ohm_0402 → +3VALW_PGPPG
			→ U13 EN.LAN_PWR_ON	→ +3V_LAN	
			→ RC173 0ohm_0402	→ +3VALW_DSW	
+19VB			→ U9 EN.WLAN_ON	→ +3VS_WLAN	
			→ U52 EN.3G_PWR_ON#	→ +3VS_3G	
			→ R5193 0ohm_0402	→ +3VALW_PD	
			→ R742 0ohm_0603	→ +3VALW_TPM	
			→ U61 EN.PM_SLP_A#	→ +3VM	→ RC154 0ohm → +3VALW_SPI
+19VB			→ PU502 EN.SYSON	→ +2.5V	
			→ PU701 EN.SPOK	→ +1.8VALW_PRIM	→ JPC8 JUMP → +1.8VALW_VS → UC5 EN.SUSP# → +1.8VS → LC2 → +1.8VS_VDDA
			→ U5008 EN.SUSP#	→ +3VS	→ U8 EN.SOC_ENVDD → +LCDVDD
				→ L3	→ +3VS_CRT
				→ R640 0ohm_0603	→ +3V_NFC
+19VB				→ J13 JUMP	→ +3VS_SSD_NGFF
				→ LC4	→ +3VS_DVDD
				→ LC10	→ +3VS_DMC
				→ R661 0ohm_0402	→ +3V_USB
			→ R1679 0ohm_0603	→ +3VS_TBT	→ R1582 0ohm_0603 → +3.3V_TBT_SX
+19VB			→ R741 0ohm_0603	→ +3VS_TPM	
			→ U12 EN.DGPU_PWR_E	→ +3VSDGPU_AON	→ R213 0ohm_0805 → +3VSDGPU_MAIN
			→ PU1101 EN.DGPU_PWRON	→ +1.95VSDGPU	

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				Rev	0.2

PWR Sequence_SKL-U2+2_DDR4_Value_NON CS

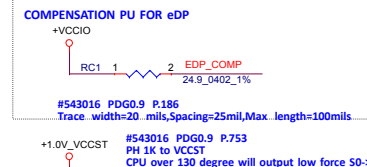


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				Custom	LA-D301P
				Date:	Thursday, December 17, 2015
				Sheet	5 of 63
				Rev	0.2

Functional Strap Definitions

#543016 PDG0.9 P.775

DDPB_CTRLDATA/ GPP_E19 (Internal Pull Down):
DDPC_CTRLDATA/ GPP_E21 (Internal Pull Down):
DDPD_CTRLDATA/ GPP_E23 (Internal Pull Down):
(Sampled:Rising edge of PCH_PWROK)
Display Port B/C/D Detected
0 =Port is not detected.
1 =Port is detected.



#543016 PDG0.9 P.186
Trace width=20 mils,Spacing=25mil,Max length=100mils
AR HDMI D08

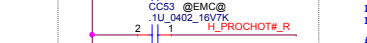
#543016 PDG0.9 P.753
PH 1K to VCCST
CPU over 130 degree will output low force 50>55



#543016 PDG0.9 P.771
PROC_POPIRCOMP/PCH_OPIRCOMP
PD 50ohm



#544669 CRB RVP7 1.0
EDRAM_OPIO_RCOMP/EOPIO_RCOMP
PD50ohm



Reserved for ESD 2014/9/17



Place to CPU side



Place to CPU side



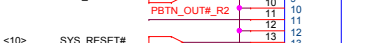
Follow 544924_SkyLake_EDS_Vol_1_Rev_0.93



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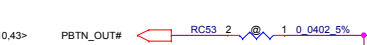
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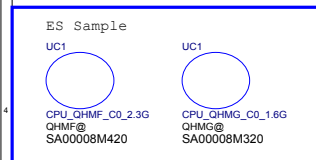
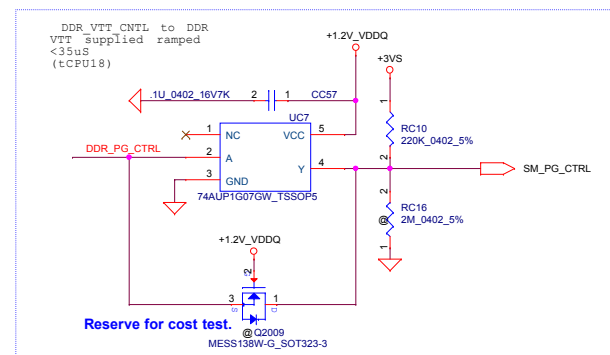
Place to CPU side

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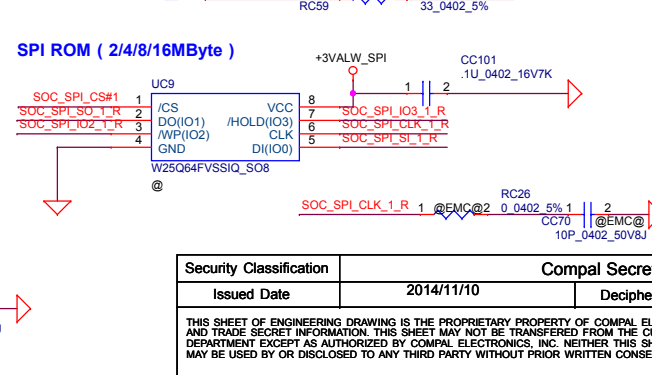
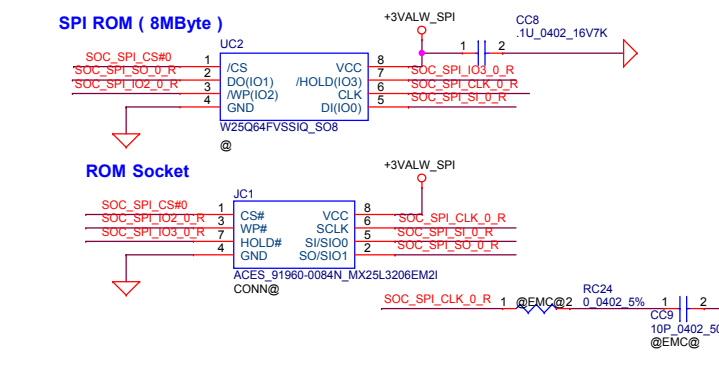
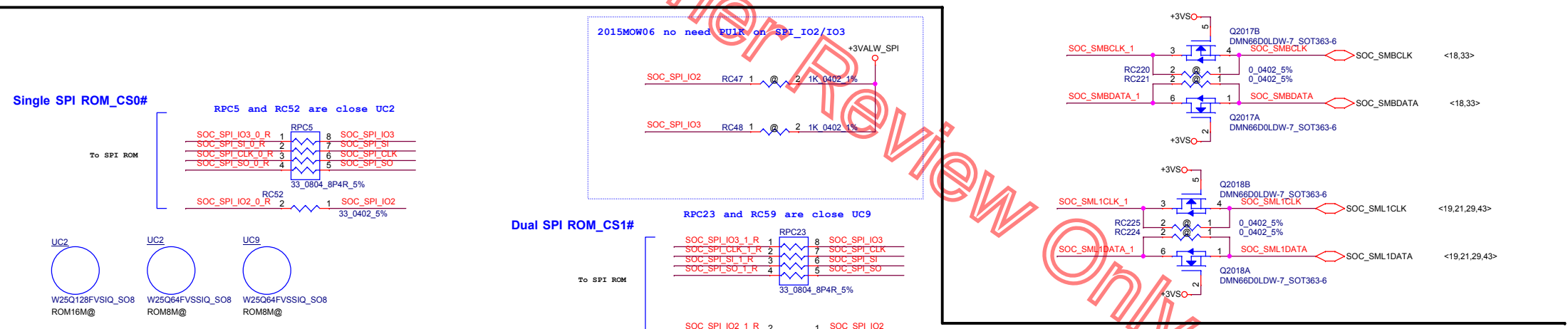
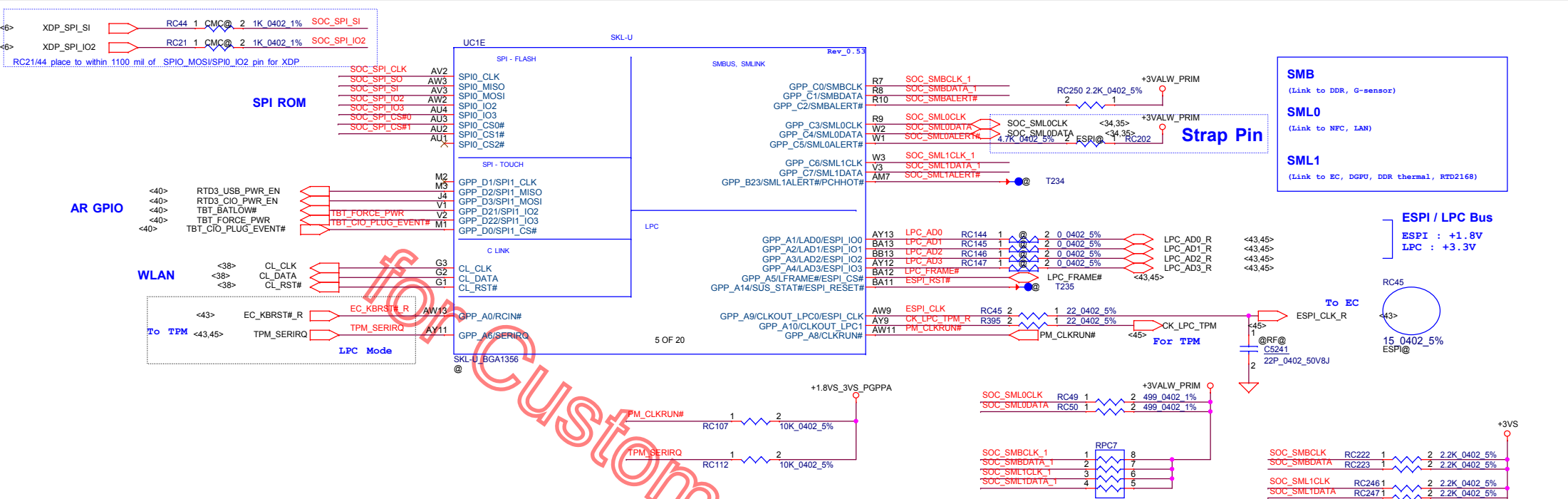
Place to CPU side

Place to CPU side

Interleaved Memory



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SPI ROM Setting	Bom Option
8M + 2M (Standard Demand)	Single SPI = 2M_SINGLE@(UC2) Dual SPI = 8M_DUAL@
8M + 4M(If Support ISH)	Single = 4M_SINGLE@(UC2) Dual SPI = 8M_DUAL@
8M + 8M(If Support ISH+VPRO)	Single = 8M_SINGLE@(UC2) Dual SPI = 8M_DUAL@
16M	Single = 16M_SINGLE@ (UC2)

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Title			Compal Electronics, Inc.		
Document Number			SKL-U(3/12)SPI,ESPI,SMB,LPC		
Date			Thursday, December 17, 2015		
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11.7.3 Intel HD Audio link capabilities

- Two SDI signals to support two external codecs.
- Drives variable frequency (6 MHz to 24 MHz) BCLK to support:
 - SDO double pumped up to 48 Mb/s
 - SDI's single pumped up to 24 Mb/s
- Provides cadence for 44.1 kHz-based sample rate output.
- Supports 1.5V, 1.8V and 3.3V modes.

Functional Strap Definitions

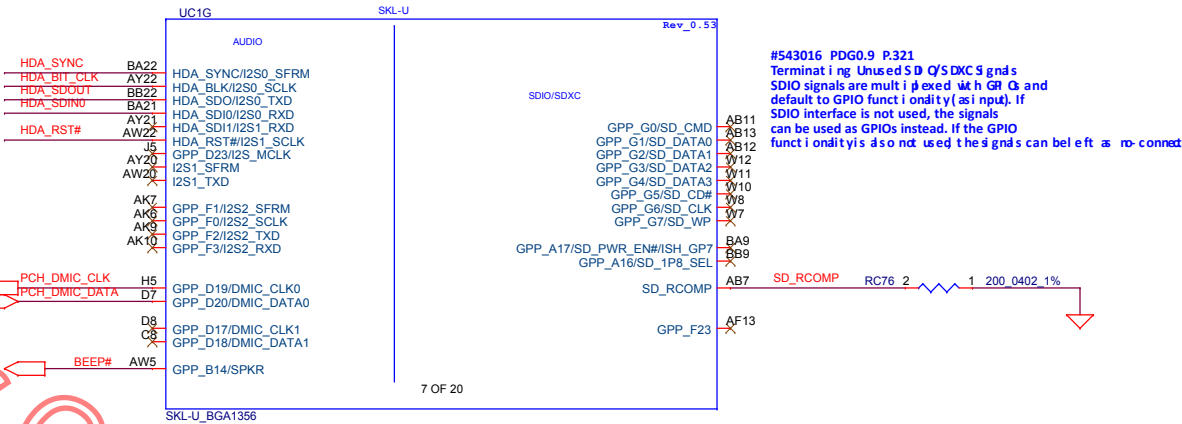
SPKR / GPP_B14 (Internal Pull Down):
(Sampled) Rising edge of PCH_PWROK)

TOP Swap Override
0 = Disable TOP Swap mode.----> AAX05 Use
1 = Enable TOP Swap Mode.

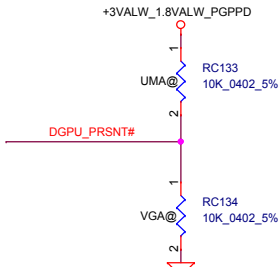
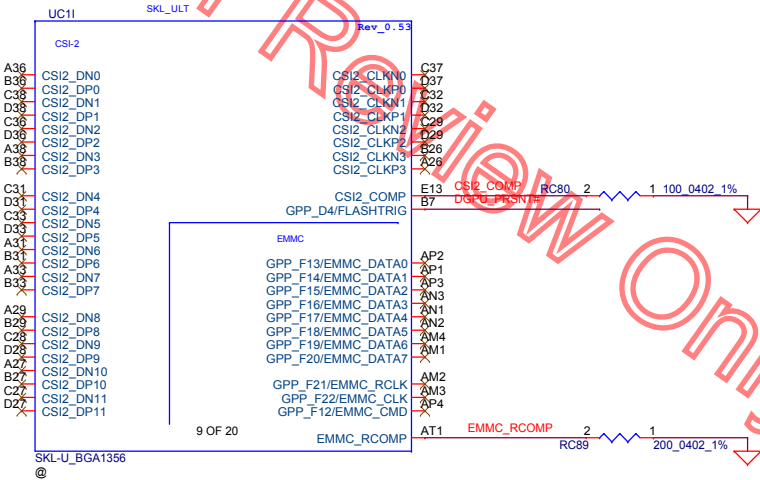
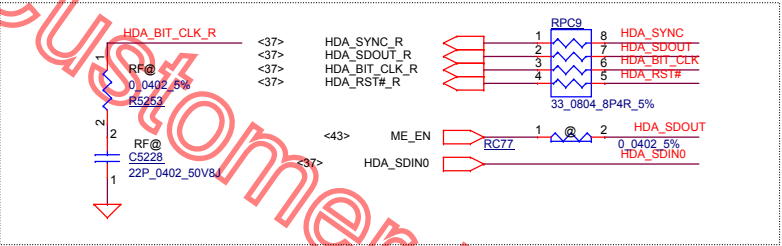
62.3.38 RCOMP Checklist

Table 62-48. RCOMP Checklist

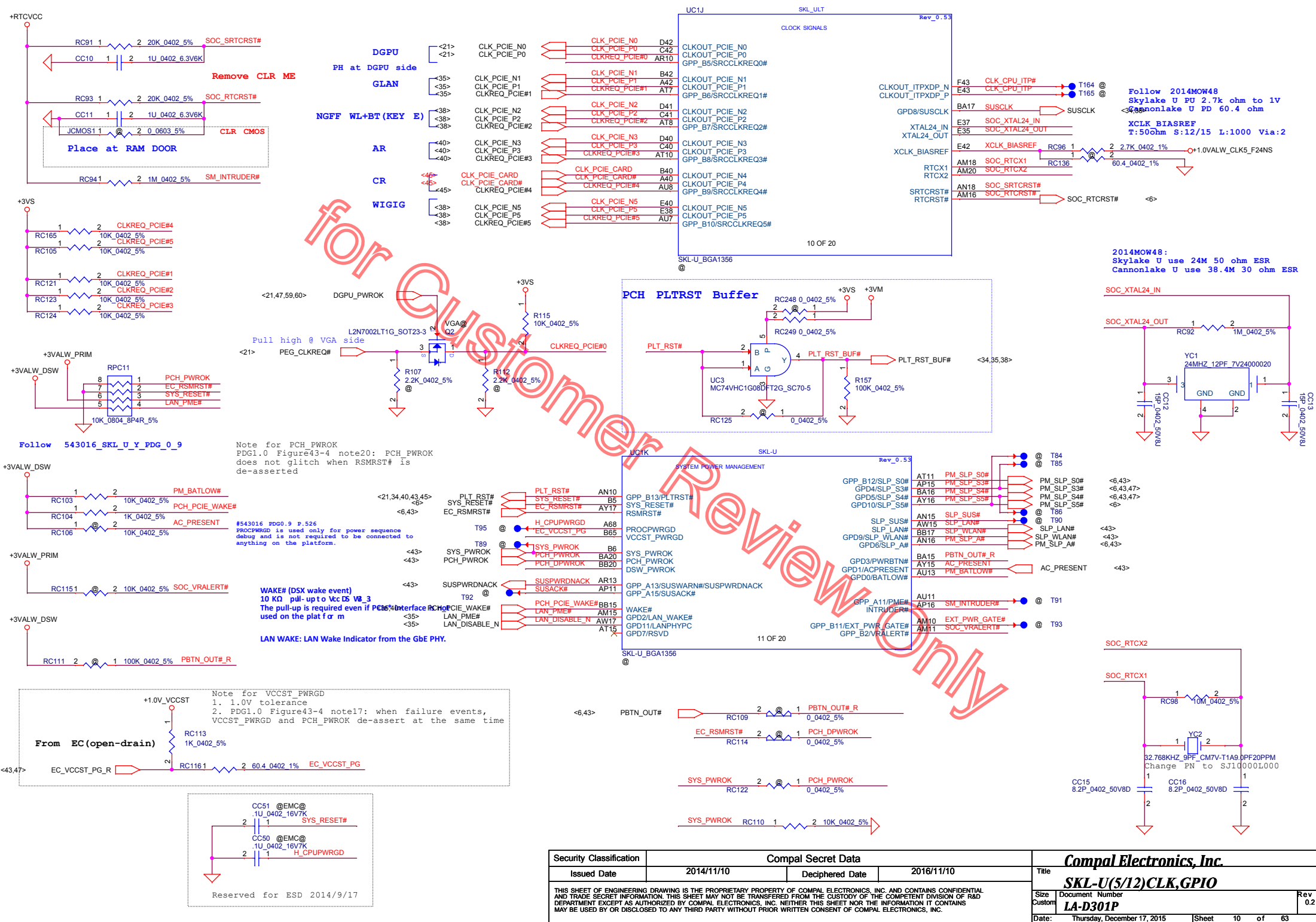
Component	Value	✓
NOA_RCOMP	49.9 ohm +/- 1% pull down termination to GND	
PEG_COMP	24.9ohm +/- 1% pull down termination to GND	
SD_RCOMP	200ohms termination to GND.	
EHMC_RCOMP	200ohms termination to GND.	
PCIE_RCOMP/N	100 ohm +/- 1%. Differential between RCOMP/RCOMP	
USB2_COMP	113 Ohm +/- 1% differential termination to GND; DC resistance <0.5ohm.	
SD_RCOMP	200ohms termination to GND.	
EHMC_RCOMP	200ohms termination to GND.	
PCH_POPIRCOMP	DC resistance <0.2ohm. 49.9 ohm termination resistor to GND.	
PCIE_RCOMP/N	100 ohm +/- 1%. Differential between RCOMP/RCOMP	
CSI2_COMP	100 ohm +/- 1% termination resistor to GND; DC resistance <0.5ohm.	
USB2_COMP	113 Ohm +/- 1% differential termination to GND; DC resistance <0.5ohm.	



HDA for AUDIO

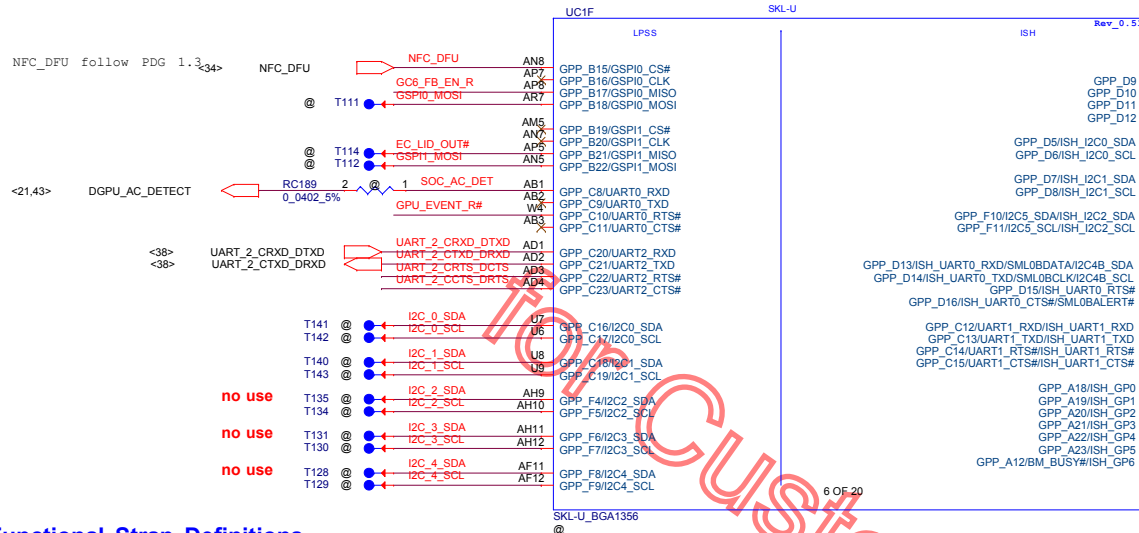


	GPIO67 DGPU_PRSN#
DIS,Optimus	0
UMA	1



Security Classification		Compal Secret Data		Compal Electronics, Inc.					
Issued Date	2014/11/10	Deciphered Date	2016/11/10	Title	SKL-U(5/12)CLK,GPIO				
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The sensors are connected to ISH through ISH I2C interface and ISH GPIO. Sensors can be connected to ISH_I2C0 or ISH_I2C1, but not to ISH_I2C2 as it is used for other function.



ISH sensor HUB
(Reserve for Verify)

no use

no use

Functional Strap Definitions

SPKR / GPP_B14 (Internal Pull Down):
(Sampled: Rising edge of PCH_PWROK)

TOP Swap Override
 * 0 = Disable TOP Swap mode. --> AAX05 Use
 1 = Enable TOP Swap Mode.

GSPI0_MOSI / GPP_B18 (Internal Pull Down):
(Rising edge of PCH_PWROK)
No Reboot

* 0 = Disable No Reboot mode. --> AAX05 Use
 1 = Enable No Reboot Mode. (PCH will disable the TCO Timer system reboot feature). This function is useful when running ITP/XDP.

GSPI1_MOSI / GPP_B22 (Internal Pull Down):
(Rising edge of PCH_PWROK)

Boot BIOS Strap Bit
 * 0 = SPI Mode --> AAX05 Use
 1 = LPC Mode

SML0ALERT# / GPP_C5 (Internal Pull Down):
(Sampled: Rising edge of RSMRST#)

eSPI or LPC
 * 0 = LPC is selected for EC --> For KB9022/9032 Use
 1 = eSPI is selected for EC --> For KB9032 Only.

SMBALERT# / GPP_C2 (Internal Pull Down):
(Sampled: Rising edge of RSMRST#)

TLS Confidentiality
 * 0 = Disable Intel ME Crypto Transport Layer Security (TLS) cipher suite (no confidentiality).
 1 = Enable Intel ME Crypto (TLS) (with confidentiality).
 Must be pulled up to support Intel AMT with TLS and Intelpull-up in manufacturing/debug environments ONLY.
 SBA (Small Business Advantage) with TLS.

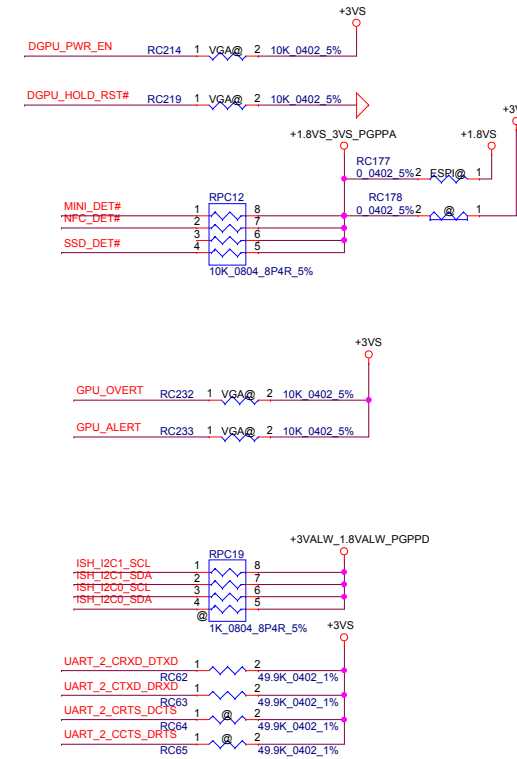
HDA_SDO/I2S_TXD0 (Internal Pull Down):
(Sampled: Rising edge of PCH_PWROK)
Flash Descriptor Security Override
 0 = Enable security measures defined in the Flash Descriptor.
 1 = Disable Flash Descriptor Security (override). This strap should only be asserted high using external strap pulled up in manufacturing/debug environments ONLY.

DDPB_CTRLDATA/ GPP_E19 (Internal Pull Down):
 DDPC_CTRLDATA/ GPP_E21 (Internal Pull Down):
 DDPD_CTRLDATA/ GPP_E23 (Internal Pull Down):
(Sampled: Rising edge of PCH_PWROK)
Display Port B/C/D Detected
 0 =Port D is not detected.
 1 =Port D is detected.

VGA_ID	GPP_D9
GL	0
GM	1

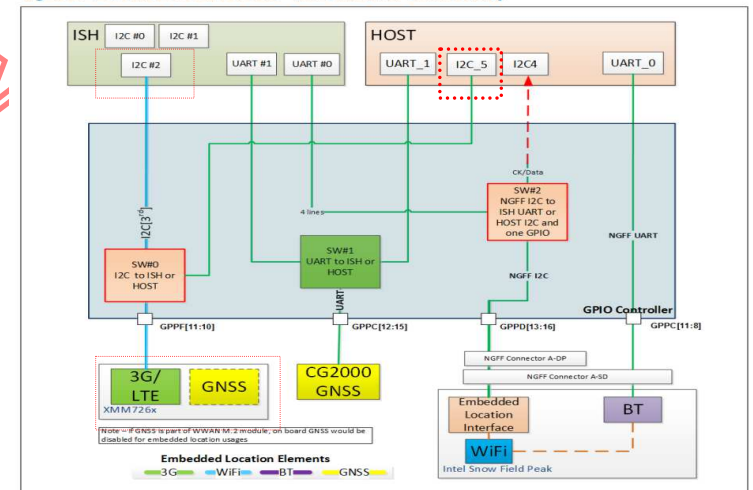
RANK_ID	GPP_D10
DR	0
SR	1

Project ID	Project_ID1 GPP_D12	Project_ID0 GPP_D11
*B4DBU+VPRO	0	0
B4DBU+NVPPO	0	1
Reserved	1	0
Reserved	1	1



I2C/ISH Port(From PDG 0.9)

Figure 64-1. Embedded Location - Host and ISH Connectivity



DGPU

GLAN

NGFF WLAN+BT (Key E)

HDD

Wigig

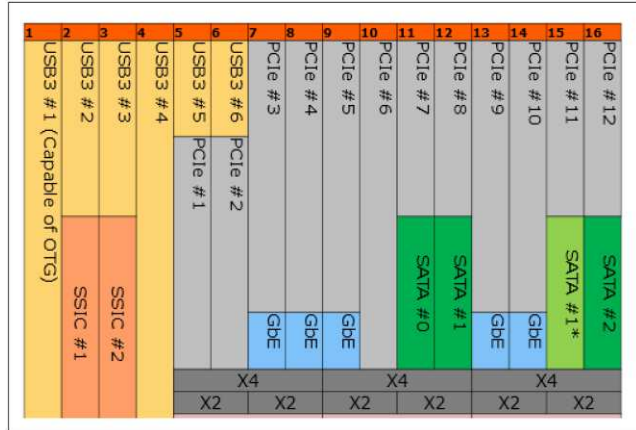
Thunderbolt

#543016 P.239 PCIE RCOMP/PCIE_RCOMP
BO=4 W=12 S=12 R=100ohm

CR

SSD

High Speed I/O (HSIO) Lane Multiplexing in SKL-U



Acer HSIQ def i ne

3.3 Intel SKYLAKE one chip.

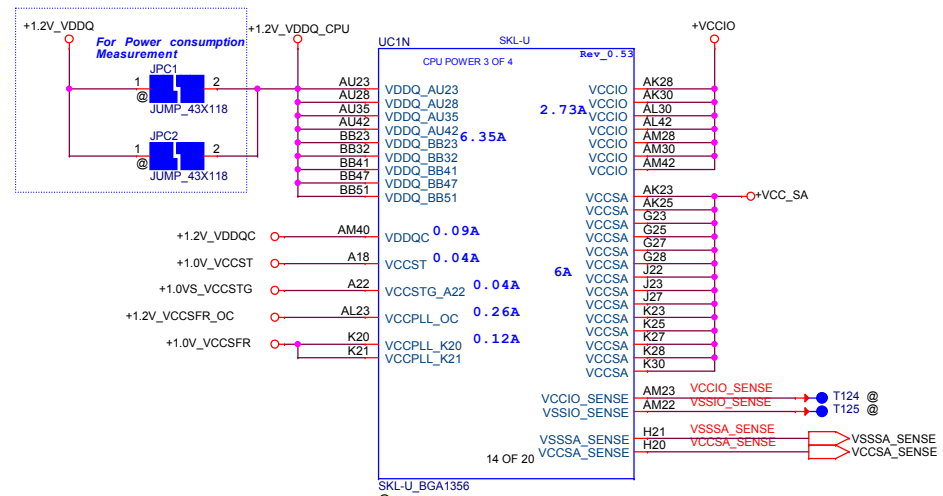
Intel		Acer 2015		SABU/MBDB	
Lane1	USB3 Port0	USB3 Port0	USB3 Port0	IO/B	
Lane2	USB3 Port0	USB3 Port0	USB3 Port0	IO/B	
Lane3	USB3 Port0	USB3 Port0	USB3 Port0	IO/B	
Lane4	USB3 Port0	USB3 Port0	USB3 Port0	IO/B	
Lane5	USB3 Port0	USB3 Port0	USB3 Port0	IO/B	
Lane6	USB3 Port0	USB3 Port0	USB3 Port0	IO/B	
Lane7	USB3 Port0	USB3 Port0	USB3 Port0	IO/B	
Lane8	USB3 Port0	USB3 Port0	USB3 Port0	IO/B	
Lane9	USB3 Port0	USB3 Port0	USB3 Port0	IO/B	
Lane10	SATA0 (Base/Preempt)	SATA0 (Base/Preempt)	SATA0 (Base/Preempt)	DOCKING	
Lane11	SATA0 (Base/Preempt)	SATA0 (Base/Preempt)	SATA0 (Base/Preempt)	DOCKING	
Lane12	SATA0 (Base/Preempt)	SATA0 (Base/Preempt)	SATA0 (Base/Preempt)	DOCKING	
Lane13	SATA0 (Base/Preempt)	SATA0 (Base/Preempt)	SATA0 (Base/Preempt)	DOCKING	
Lane14	SATA0 (Base/Preempt)	SATA0 (Base/Preempt)	SATA0 (Base/Preempt)	DOCKING	
Lane15	SATA0 (Base/Preempt)	SATA0 (Base/Preempt)	SATA0 (Base/Preempt)	DOCKING	
Lane16	SATA0 (Base/Preempt)	SATA0 (Base/Preempt)	SATA0 (Base/Preempt)	DOCKING	
Lane17	SATA0 (Base/Preempt)	SATA0 (Base/Preempt)	SATA0 (Base/Preempt)	DOCKING	
Lane18	SATA0 (Base/Preempt)	SATA0 (Base/Preempt)	SATA0 (Base/Preempt)	DOCKING	
Lane19	SATA0 (Base/Preempt)	SATA0 (Base/Preempt)	SATA0 (Base/Preempt)	DOCKING	
Lane20	SATA0 (Base/Preempt)	SATA0 (Base/Preempt)	SATA0 (Base/Preempt)	DOCKING	
Lane21	SATA0 (Base/Preempt)	SATA0 (Base/Preempt)	SATA0 (Base/Preempt)	DOCKING	
Lane22	SATA0 (Base/Preempt)	SATA0 (Base/Preempt)	SATA0 (Base/Preempt)	DOCKING	
Lane23	SATA0 (Base/Preempt)	SATA0 (Base/Preempt)	SATA0 (Base/Preempt)	DOCKING	
Lane24	SATA0 (Base/Preempt)	SATA0 (Base/Preempt)	SATA0 (Base/Preempt)	DOCKING	
Lane25	SATA0 (Base/Preempt)	SATA0 (Base/Preempt)	SATA0 (Base/Preempt)	DOCKING	
Lane26	SATA0 (Base/Preempt)	SATA0 (Base/Preempt)	SATA0 (Base/Preempt)	DOCKING	
Lane27	SATA0 (Base/Preempt)	SATA0 (Base/Preempt)	SATA0 (Base/Preempt)	DOCKING	
Lane28	SATA0 (Base/Preempt)	SATA0 (Base/Preempt)	SATA0 (Base/Preempt)	DOCKING	
Lane29	SATA0 (Base/Preempt)	SATA0 (Base/Preempt)	SATA0 (Base/Preempt)	DOCKING	
Lane30	SATA0 (Base/Preempt)	SATA0 (Base/Preempt)	SATA0 (Base/Preempt)	DOCKING	
Lane31	SATA0 (Base/Preempt)	SATA0 (Base/Preempt)	SATA0 (Base/Preempt)	DOCKING	
Lane32	SATA0 (Base/Preempt)	SATA0 (Base/Preempt)	SATA0 (Base/Preempt)	DOCKING	
Lane33	SATA0 (Base/Preempt)	SATA0 (Base/Preempt)	SATA0 (Base/Preempt)	DOCKING	
Lane34	SATA0 (Base/Preempt)	SATA0 (Base/Preempt)	SATA0 (Base/Preempt)	DOCKING	
Lane35	SATA0 (Base/Preempt)	SATA0 (Base/Preempt)	SATA0 (Base/Preempt)	DOCKING	
Lane36	SATA0 (Base/Preempt)	SATA0 (Base/Preempt)	SATA0 (Base/Preempt)	DOCKING	
Lane37	SATA0 (Base/Preempt)	SATA0 (Base/Preempt)	SATA0 (Base/Preempt)	DOCKING	
Lane38	SATA0 (Base/Preempt)	SATA0 (Base/Preempt)	SATA0 (Base/Preempt)	DOCKING	
Lane39	SATA0 (Base/Preempt)	SATA0 (Base/Preempt)	SATA0 (Base/Preempt)	DOCKING	
Lane40	SATA0 (Base/Preempt)	SATA0 (Base/Preempt)	SATA0 (Base/Preempt)	DOCKING	
Lane41	SATA0 (Base/Preempt)	SATA0 (Base/Preempt)	SATA0 (Base/Preempt)	DOCKING	
Lane42	SATA0 (Base/Preempt)	SATA0 (Base/Preempt)	SATA0 (Base/Preempt)	DOCKING	
Lane43	SATA0 (Base/Preempt)	SATA0 (Base/Preempt)	SATA0 (Base/Preempt)	DOCKING	
Lane44	SATA0 (Base/Preempt)	SATA0 (Base/Preempt)	SATA0 (Base/Preempt)	DOCKING	
Lane45	SATA0 (Base/Preempt)	SATA0 (Base/Preempt)	SATA0 (Base/Preempt)	DOCKING	
Lane46	SATA0 (Base/Preempt)	SATA0 (Base/Preempt)	SATA0 (Base/Preempt)	DOCKING	
Lane47	SATA0 (Base/Preempt)	SATA0 (Base/Preempt)	SATA0 (Base/Preempt)	DOCKING	
Lane48	SATA0 (Base/Preempt)	SATA0 (Base/Preempt)	SATA0 (Base/Preempt)	DOCKING	
Lane49	SATA0 (Base/Preempt)	SATA0 (Base/Preempt)	SATA0 (Base/Preempt)	DOCKING	
Lane50	SATA0 (Base/Preempt)	SATA0 (Base/Preempt)	SATA0 (Base/Preempt)	DOCKING	
Lane51	SATA0 (Base/Preempt)	SATA0 (Base/Preempt)	SATA0 (Base/Preempt)	DOCKING	
Lane52	SATA0 (Base/Preempt)	SATA0 (Base/Preempt)	SATA0 (Base/Preempt)	DOCKING	
Lane53	SATA0 (Base/Preempt)	SATA0 (Base/Preempt)	SATA0 (Base/Preempt)	DOCKING	
Lane54	SATA0 (Base/Preempt)	SATA0 (Base/Preempt)	SATA0 (Base/Preempt)	DOCKING	
Lane55	SATA0 (Base/Preempt)	SATA0 (Base/Preempt)	SATA0 (Base/Preempt)	DOCKING	
Lane56	SATA0 (Base/Preempt)	SATA0 (Base/Preempt)	SATA0 (Base/Preempt)	DOCKING	
Lane57	SATA0 (Base/Preempt)	SATA0 (Base/Preempt)	SATA0 (Base/Preempt)	DOCKING	
Lane58	SATA0 (Base/Preempt)	SATA0 (Base/Preempt)	SATA0 (Base/Preempt)	DOCKING	
Lane59	SATA0 (Base/Preempt)	SATA0 (Base/Preempt)	SATA0 (Base/Preempt)	DOCKING	
Lane60	SATA0 (Base/Preempt)	SATA0 (Base/Preempt)	SATA0 (Base/Preempt)	DOCKING	
Lane61	SATA0 (Base/Preempt)	SATA0 (Base/Preempt)	SATA0 (Base/Preempt)	DOCKING	
Lane62	SATA0 (Base/Preempt)	SATA0 (Base/Preempt)	SATA0 (Base/Preempt)	DOCKING	
Lane63	SATA0 (Base/Preempt)	SATA0 (Base/Preempt)	SATA0 (Base/Preempt)	DOCKING	
Lane64	SATA0 (Base/Preempt)	SATA0 (Base/Preempt)	SATA0 (Base/Preempt)	DOCKING	
Lane65	SATA0 (Base/Preempt)	SATA0 (Base/Preempt)	SATA0 (Base/Preempt)	DOCKING	
Lane66	SATA0 (Base/Preempt)	SATA0 (Base/Preempt)	SATA0 (Base/Preempt)	DOCKING	
Lane67	SATA0 (Base/Preempt)	SATA0 (Base/Preempt)	SATA0 (Base/Preempt)	DOCKING	
Lane68	SATA0 (Base/Preempt)	SATA0 (Base/Preempt)	SATA0 (Base/Preempt)	DOCKING	
Lane69	SATA0 (Base/Preempt)	SATA0 (Base/Preempt)	SATA0 (Base/Preempt)	DOCKING	
Lane70	SATA0 (Base/Preempt)	SATA0 (Base/Preempt)	SATA0 (Base/Preempt)	DOCKING	
Lane71	SATA0 (Base/Preempt)	SATA0 (Base/Preempt)	SATA0 (Base/Preempt)	DOCKING	
Lane72	SATA0 (Base/Preempt)	SATA0 (Base/Preempt)	SATA0 (Base/Preempt)	DOCKING	
Lane73	SATA0 (Base/Preempt)	SATA0 (Base/Preempt)	SATA0 (Base/Preempt)	DOCKING	
Lane74	SATA0 (Base/Preempt)	SATA0 (Base/Preempt)	SATA0 (Base/Preempt)	DOCKING	
Lane75	SATA0 (Base/Preempt)	SATA0 (Base/Preempt)	SATA0 (Base/Preempt)	DOCKING	
Lane76	SATA0 (Base/Preempt)	SATA0 (Base/Preempt)	SATA0 (Base/Preempt)	DOCKING	
Lane77	SATA0 (Base/Preempt)	SATA0 (Base/Preempt)	SATA0 (Base/Preempt)	DOCKING	
Lane78	SATA0 (Base/Preempt)	SATA0 (Base/Preempt)	SATA0 (Base/Preempt)	DOCKING	
Lane79	SATA0 (Base/Preempt)	SATA0 (Base/Preempt)	SATA0 (Base/Preempt)	DOCKING	
Lane80	SATA0 (Base/Preempt)	SATA0 (Base/Preempt)	SATA0 (Base/Preempt)	DOCKING	
Lane81	SATA0 (Base/Preempt)	SATA0 (Base/Preempt)	SATA0 (Base/Preempt)	DOCKING	
Lane82	SATA0 (Base/Preempt)	SATA0 (Base/Preempt)	SATA0 (Base/Preempt)	DOCKING	
Lane83	SATA0 (Base/Preempt)	SATA0 (Base/Preempt)	SATA0 (Base/Preempt)	DOCKING	
Lane84	SATA0 (Base/Preempt)	SATA0 (Base/Preempt)	SATA0 (Base/Preempt)	DOCKING	
Lane85	SATA0 (Base/Preempt)	SATA0 (Base/Preempt)	SATA0 (Base/Preempt)	DOCKING	
Lane86	SATA0 (Base/Preempt)	SATA0 (Base/Preempt)	SATA0 (Base/Preempt)	DOCKING	
Lane87	SATA0 (Base/Preempt)	SATA0 (Base/Preempt)	SATA0 (Base/Preempt)	DOCKING	
Lane88	SATA0 (Base/Preempt)	SATA0 (Base/Preempt)	SATA0 (Base/Preempt)	DOCKING	
Lane89	SATA0 (Base/Preempt)	SATA0 (Base/Preempt)	SATA0 (Base/Preempt)	DOCKING	
Lane90	SATA0 (Base/Preempt)	SATA0 (Base/Preempt)	SATA0 (Base/Preempt)	DOCKING	
Lane91	SATA0 (Base/Preempt)	SATA0 (Base/Preempt)	SATA0 (Base/Preempt)	DOCKING	
Lane92	SATA0 (Base/Preempt)	SATA0 (Base/Preempt)	SATA0 (Base/Preempt)	DOCKING	
Lane93	SATA0 (Base/Preempt)	SATA0 (Base/Preempt)	SATA0 (Base/Preempt)	DOCKING	
Lane94	SATA0 (Base/Preempt)	SATA0 (Base/Preempt)	SATA0 (Base/Preempt)	DOCKING	
Lane95	SATA0 (Base/Preempt)	SATA0 (Base/Preempt)	SATA0 (Base/Preempt)	DOCKING	
Lane96	SATA0 (Base/Preempt)	SATA0 (Base/Preempt)	SATA0 (Base/Preempt)	DOCKING	
Lane97	SATA0 (Base/Preempt)	SATA0 (Base/Preempt)	SATA0 (Base/Preempt)	DOCKING	
Lane98	SATA0 (Base/Preempt)	SATA0 (Base/Preempt)	SATA0 (Base/Preempt)	DOCKING	
Lane99	SATA0 (Base/Preempt)	SATA0 (Base/Preempt)	SATA0 (Base/Preempt)	DOCKING	
Lane100	SATA0 (Base/Preempt)	SATA0 (Base/Preempt)	SATA0 (Base/Preempt)	DOCKING	

GPIO		DEVICE CONTROL	
USB_OC0#	NA	USB2 Port 1,2,4	
USB_OC1#	NA		
USB_OC2#	NA		
USB_OC3#	NA		
DEVSLP0	NA		
DEVSLP1	SSD		
DEVSLP2	NA		
SATA_GP0	NA		
SATA_GP1	NA		
SATA_GP2	NA		

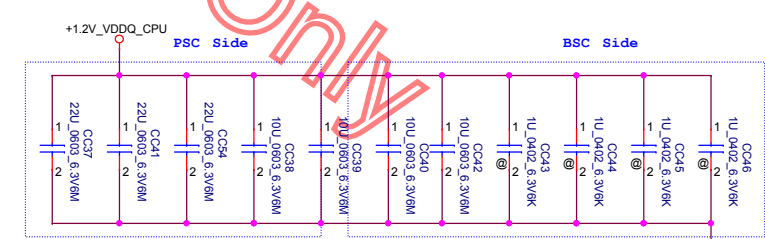
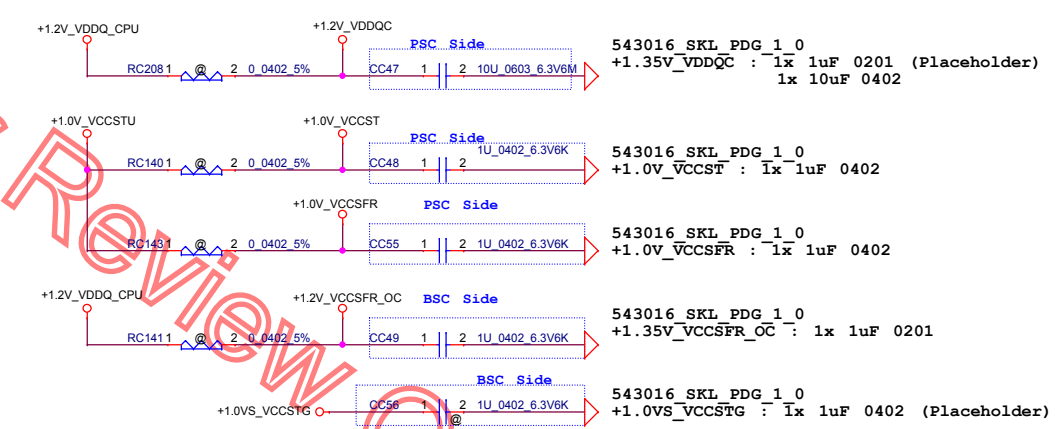
DEVSLP[2:0] Implementation
DEVSLP is a host-controlled hardware signal which enables a SATA host and device to enter an ultra-low interface power state, including the possibility to completely power down host and device PHYs.
The processor provides three SATA DEVSLP signals, DEVSLP[2:0] for SKL-U.
When high, DEVSLP requests the SATA device to enter into the DEVSLP power state.
When low, DEVSLP requests the SATA device to exit from the DEVSLP power state and transition to active state.

SATA General Purpose (SATAGP[2:0]) Signals
The processor provides three SATA general purpose input signals, SATAGP[2:0] for SKL-U. These signals can be configured as interlock switch inputs corresponding to a given SATA port. When used as an interlock switch status indication, this signal should be driven to 0 to indicate that the switch is closed and to a 1 to indicate that the switch is open.
If mechanical presence switches will not be used on the platform, SATAGP[2:0] signals can be configured as GPP_E[2:0] GPIOs signals.

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Issued Date	2014/11/10	Deciphered Date	2016/11/10	Title	SKL-U(7/12)PCIE,USB,SATA
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				Custom	LA-D301P
				Date	Thursday, December 17, 2015
				Sheet	12 of 63
				Rev	0.2

[illegible]

VCCSTG and VCCIO SLEW RATE <=65us



The diagram illustrates the power supply section of the BSC and PSC boards. It shows a +VCCIO input connected to a series of capacitors (C227, C228, C229, C230, C231, C232, C233, C234, C235, C236) connected in parallel to ground. The capacitors are labeled with their values: C227 (10U, 0.003, 6.3V6M), C228 (10U, 0.003, 6.3V6M), C229 (11U, 0.042, 6.3V6K), C230 (11U, 0.042, 6.3V6K), C231 (11U, 0.042, 6.3V6K), C232 (11U, 0.042, 6.3V6K), C233 (11U, 0.042, 6.3V6K), C234 (11U, 0.042, 6.3V6K), C235 (11U, 0.042, 6.3V6K), and C236 (11U, 0.042, 6.3V6K). The diagram is divided into two sections: BSC Side and PSC Side.

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				Date:	Thursday, December 17, 2015	Sheet

#544924 Skylake EDS P.125

7.2.1.6 VCC_{OPC} DC Specifications

VCC_{OPC} is fixed OPC VR output voltage of 1V. The processor can drive VR to LPM (Low Power Mode) which uses VR output to DV using ZVRR signal as shown below:

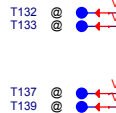
Table 7-5. VCC _{OPC} Voltage Levels			
ZVRR state	VCC _{OPC}	VR	Units
1	1	1	V
1	1	1	V

VCC _{OPC} Voltage Levels (separate VR)			
ZVRR state	VR state	VCC _{OPC}	Units
0	0	0	V
1	0	0	V
1	1	1.0	V

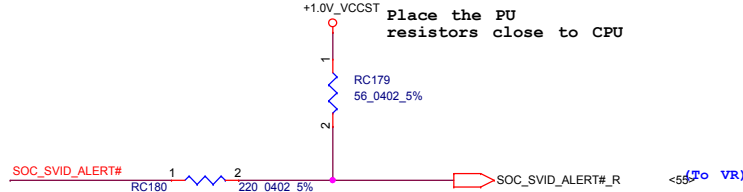
Notes:
1. Processor VR doesn't support input signal.

#544924 Skylake EDS P.125
VCC_{OPC} 1V 2.8A
VCC_{OPC} 1P8 1.8V 50mA
VCC_{EOPIO} 0V,0.8V,1V 2.9A

For CPU2+3e SKU



SVID ALERT



SVID DATA

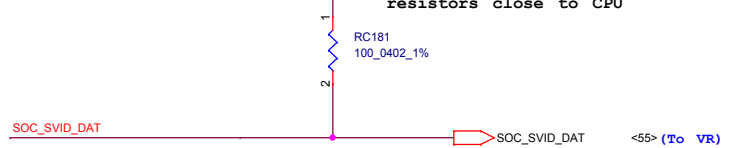


Table 2-1.

Package Sensing Recommendations			
Power Rail Sense Line	R1, R2	Trace Impedance	Trace Length Match
Vcc_SENSE / Vss_SENSE	100Ω	50Ω	<25 mils
Vcc _{OPC} _SENSE / Vss _{OPC} _SENSE			
Vcc _{GT} _SENSE / Vss _{GT} _SENSE			
Vcc _{GT} _SENSE / Vss _{GT} _SENSE			
Vcc _{GT} _SENSE / Vss _{GT} _SENSE			
Vcc _{GT} _SENSE / Vss _{GT} _SENSE	NA		

Note: [1] Does not apply when rails are merged.

To minimize any stray noise pickup to the Vcc_SENSE/Vss_SENSE lines

- Sense traces should be referenced to a solid ground plane
- Avoid crossing over plane splits
- Maintain a 25-mil separation distance away from any other dynamic signals

543016 PDG0.9 P.189 Need check

Table 10-10. SVID Bus Routing Guidelines

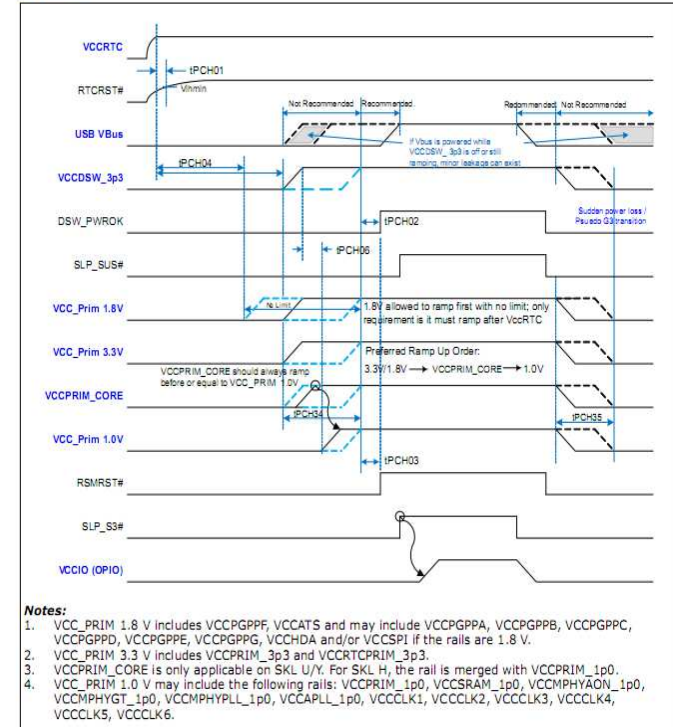
Signal	W1 [inches]	W2 [inches]	W3/4/5 [inches]	W2+W3+W4+W5 [inches]	W5 [inches]	W52 [inches]	R _{P1} [Ω]	R _{P2} [Ω]	R _{S1} [Ω]	R _{S2} [Ω]	VCC ST [V]
VIDSOUT							Empty	45	0	50	
VIDSCK	0.5-3	1-15	0.5-4	3-17	<0.1	<0.1	100	100	0	10	1.0
VIDALER T#							56	Empty	220	0	

Processor Power Rails

Power Rail	Description	Control
VCC	Processor IA Cores Power Rail	SVID
VCCGT	Processor Graphics Power Rails	SVID
VCCGTx	Processor Graphics Extended Power Rail Available only for GT3/GT4 processor SKUs	SVID
VCCSA	System Agent Power Rail	SVID/Fixed (SKU dependent)
VCCIO	IO Power Rail	Fixed
VCCGT	Sustain Power Rail	Fixed
VCCPLL	Processor PLLs power rail	Fixed
VDDQ	Integrated Memory Controller Power Rail	Fixed (Memory technology dependent)
VCCOPC	Processor OPC power rail (available only in SKU's with OPC)	Fixed
VCCOPC_1P8	Processor OPC power rail (available only in SKU's with OPC)	Fixed
VCCEOPIO	Processor EOPIO power rail (available only in SKU's with OPC)	Fixed

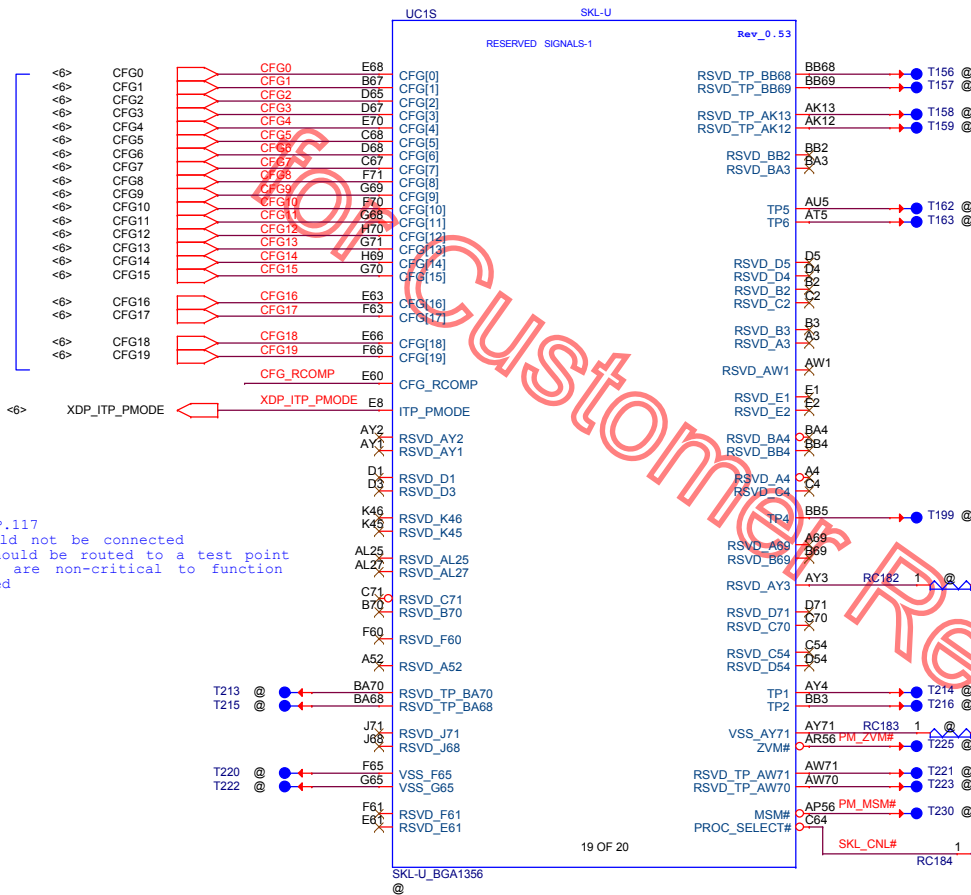
UC1P SKL-U Rev_0.53			UC1Q SKL-U Rev_0.53			UC1R SKL-U Rev_0.53		
GND 1 OF 3			GND 2 OF 3			GND 3 OF 3		
A5 VSS	AL65 VSS	AT63 VSS	BA49 VSS	F8 VSS	L18 VSS			
A67 VSS	AL66 VSS	AT68 VSS	BA53 VSS	G10 VSS	L2 VSS			
A70 VSS	AM13 VSS	AT71 VSS	BA57 VSS	G22 VSS	L20 VSS			
AA2 VSS	AM21 VSS	AU10 VSS	BA6 VSS	G43 VSS	L4 VSS			
AA4 VSS	AM25 VSS	AU15 VSS	BA62 VSS	G45 VSS	L8 VSS			
AA65 VSS	AM27 VSS	AU20 VSS	BA66 VSS	G48 VSS	N10 VSS			
AA68 VSS	AM43 VSS	AU32 VSS	BA71 VSS	G5 VSS	N13 VSS			
AB15 VSS	AM45 VSS	AU38 VSS	BB18 VSS	G52 VSS	N19 VSS			
AB16 VSS	AM46 VSS	AV1 VSS	BB26 VSS	G55 VSS	N21 VSS			
AB18 VSS	AM55 VSS	AV68 VSS	BB30 VSS	G58 VSS	N6 VSS			
AB21 VSS	AM60 VSS	AV69 VSS	BB34 VSS	G6 VSS	N65 VSS			
AB8 VSS	AM61 VSS	AV70 VSS	BB38 VSS	G60 VSS	N68 VSS			
AD13 VSS	AM68 VSS	AV71 VSS	BB43 VSS	G63 VSS	P17 VSS			
AD16 VSS	AM71 VSS	AW10 VSS	BB55 VSS	G66 VSS	P19 VSS			
AD19 VSS	AM8 VSS	AW12 VSS	BB6 VSS	H15 VSS	P20 VSS			
AD20 VSS	AN20 VSS	AW14 VSS	BB60 VSS	H18 VSS	P21 VSS			
AD21 VSS	AN23 VSS	AW16 VSS	BB64 VSS	H71 VSS	R13 VSS			
AD62 VSS	AN28 VSS	AW18 VSS	BB67 VSS	J11 VSS	R6 VSS			
AD8 VSS	AN30 VSS	AW21 VSS	BB70 VSS	J13 VSS	T15 VSS			
AE64 VSS	AN32 VSS	AW23 VSS	C1 VSS	J25 VSS	T17 VSS			
AE65 VSS	AN33 VSS	AW26 VSS	C25 VSS	J28 VSS	T18 VSS			
AE66 VSS	AN35 VSS	AW28 VSS	C5 VSS	J32 VSS	T2 VSS			
AE67 VSS	AN37 VSS	AW30 VSS	D10 VSS	J35 VSS	T21 VSS			
AE68 VSS	AN38 VSS	AW32 VSS	D11 VSS	J38 VSS	T4 VSS			
AE69 VSS	AN40 VSS	AW34 VSS	D14 VSS	J42 VSS	U10 VSS			
AF1 VSS	AN42 VSS	AW36 VSS	D18 VSS	J8 VSS	U63 VSS			
AF10 VSS	AN58 VSS	AW38 VSS	D22 VSS	K16 VSS	U64 VSS			
AF15 VSS	AN63 VSS	AW41 VSS	D25 VSS	K18 VSS	U66 VSS			
AF17 VSS	AP10 VSS	AW43 VSS	D26 VSS	K22 VSS	U67 VSS			
AF2 VSS	AP18 VSS	AW45 VSS	D30 VSS	K61 VSS	U69 VSS			
AF4 VSS	AP20 VSS	AW47 VSS	D34 VSS	K63 VSS	U70 VSS			
AF63 VSS	AP23 VSS	AW49 VSS	D39 VSS	K64 VSS	V16 VSS			
AG16 VSS	AP28 VSS	AW51 VSS	D44 VSS	K65 VSS	V17 VSS			
AG17 VSS	AP32 VSS	AW53 VSS	D45 VSS	K66 VSS	V18 VSS			
AG18 VSS	AP35 VSS	AW55 VSS	D47 VSS	K67 VSS	W13 VSS			
AG19 VSS	AP38 VSS	AW57 VSS	D48 VSS	K68 VSS	W6 VSS			
AG20 VSS	AP42 VSS	AW6 VSS	D53 VSS	K70 VSS	W9 VSS			
AG21 VSS	AP58 VSS	AW60 VSS	D58 VSS	K71 VSS	Y17 VSS			
AG71 VSS	AP63 VSS	AW62 VSS	D6 VSS	L14 VSS	Y19 VSS			
AH13 VSS	AP68 VSS	AW64 VSS	D62 VSS	L16 VSS	Y20 VSS			
AH6 VSS	AP70 VSS	AW66 VSS	D66 VSS	L17 VSS	Y21 VSS			
AH63 VSS	AR11 VSS	AW8 VSS	D69 VSS	SKL-U_BGA1356 @ 18 OF 20				
AH64 VSS	AR15 VSS	AY66 VSS	E11 VSS					
AH67 VSS	AR16 VSS	B10 VSS	E15 VSS					
AJ15 VSS	AR20 VSS	B14 VSS	E18 VSS					
AJ18 VSS	AR23 VSS	B18 VSS	E21 VSS					
AJ20 VSS	AR28 VSS	B22 VSS	E46 VSS					
AJ4 VSS	AR35 VSS	B30 VSS	E50 VSS					
AK11 VSS	AR42 VSS	B34 VSS	E53 VSS					
AK16 VSS	AR43 VSS	B39 VSS	E56 VSS					
AK18 VSS	AR45 VSS	B44 VSS	E6 VSS					
AK21 VSS	AR46 VSS	B48 VSS	E65 VSS					
AK22 VSS	AR48 VSS	B53 VSS	E71 VSS					
AK27 VSS	AR5 VSS	B58 VSS	F1 VSS					
AK63 VSS	AR50 VSS	B62 VSS	F13 VSS					
AK68 VSS	AR52 VSS	B66 VSS	F2 VSS					
AK69 VSS	AR53 VSS	B71 VSS	F22 VSS					
AK8 VSS	AR55 VSS	BA1 VSS	F23 VSS					
AL2 VSS	AR58 VSS	BA10 VSS	F27 VSS					
AL28 VSS	AR63 VSS	BA14 VSS	F28 VSS					
AL32 VSS	AR8 VSS	BA18 VSS	F32 VSS					
AL35 VSS	AT2 VSS	BA2 VSS	F33 VSS					
AL38 VSS	AT20 VSS	BA23 VSS	F35 VSS					
AL4 VSS	AT23 VSS	BA28 VSS	F37 VSS					
AL45 VSS	AT28 VSS	BA32 VSS	F38 VSS					
AL48 VSS	AT35 VSS	BA36 VSS	F4 VSS					
AL52 VSS	AT4 VSS	F68 VSS	F40 VSS					
AL55 VSS	AT42 VSS	BA45 VSS	F42 VSS					
AL59 VSS	AT56 VSS	SKL-U_BGA1356 @ 17 OF 20						
AL64 VSS	AT58 VSS							

Figure 46-18.SKL-U/Y Rail-to-Rail Sequencing Requirement for Non-Deep Sx Configured System

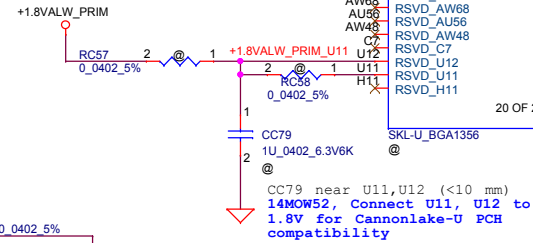


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				Size	Document Number	Rev
				Custom	LA-D301P	0.2
				Date:	Thursday, December 17, 2015	Sheet
						16 of 63

CFG Signals (For Strap & XDP)

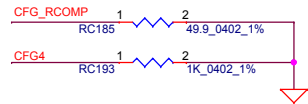


#544924 Skylake EDS 0.75 P.117
 *RSVD - these signals should not be connected
 *RSVD_TP - these signals should be routed to a test point
 *RSVD_NCTF - these signals are non-critical to function
 and may be left un-connected



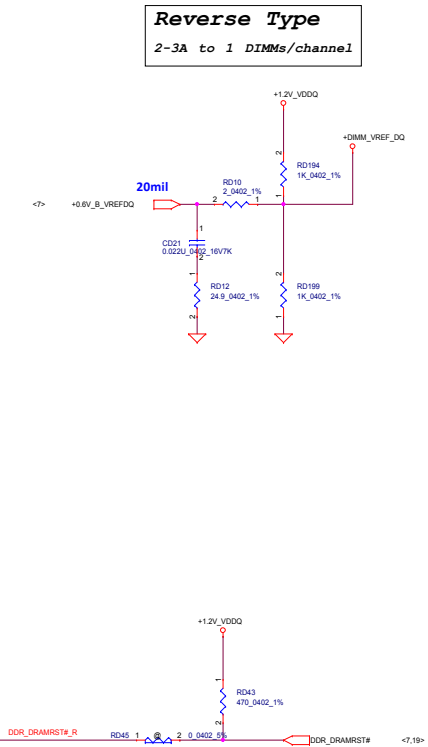
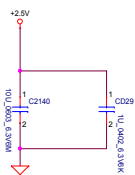
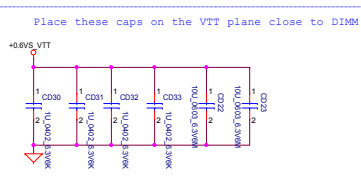
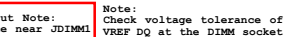
For 2+3e Solution
 PM_ZVM#
 ZeRo Voltage Mode: Control signal to OPC VR, when low OPC VR output is 0V.
 PM_MSM#
 Minimum Speed Mode: Control signal to VccEOPIO VR (connected only in 2 VR solution for OPC).
 PROC_SELECT#
 Processor Select: This pin is for compatibility with future platforms. It should NC with Skylake

Follow 544669_SKL_U_DDR3L_RVP7_schematic_rev1.0



Display Port Presence Strap	
CFG4	1 : Disabled; No Physical Display Port attached to Embedded Display Port 0 : Enabled; An external Display Port device is connected to the Embedded Display Port

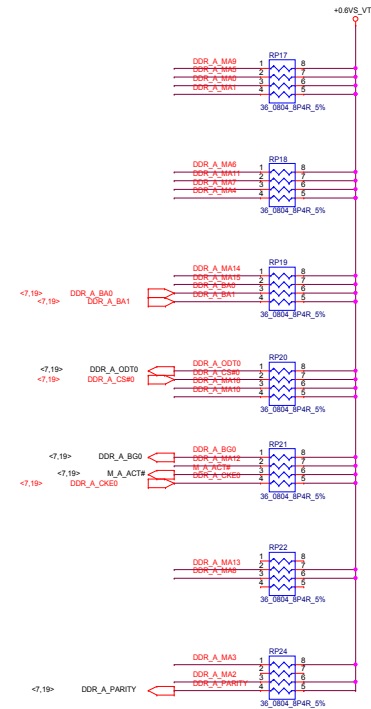
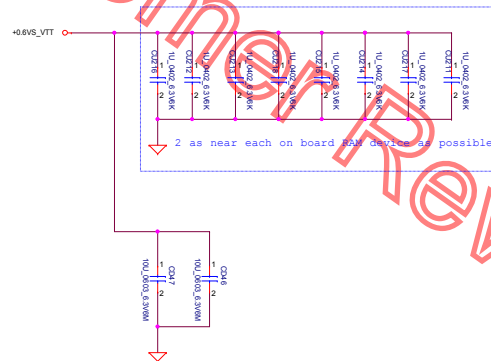
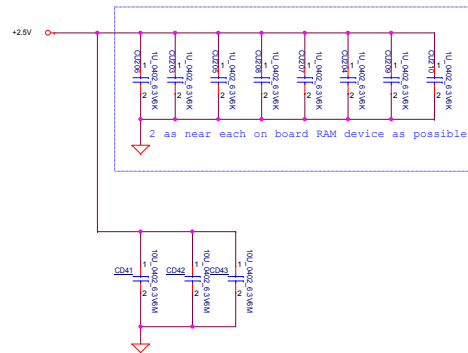
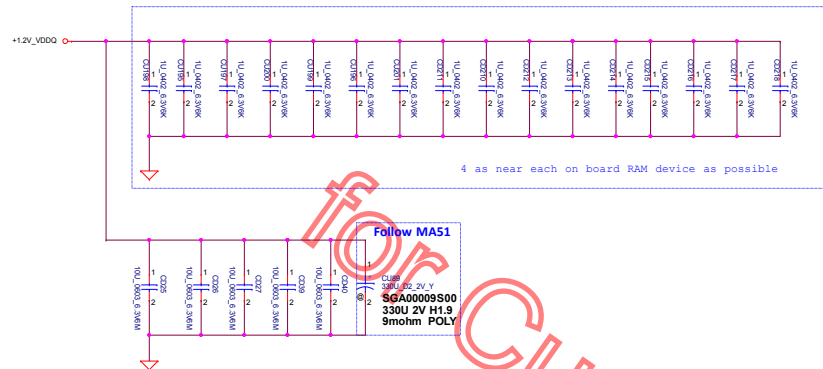
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Interleaved Memory

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<7.19> DDR_A_MA[0..16]



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VRAM Interface

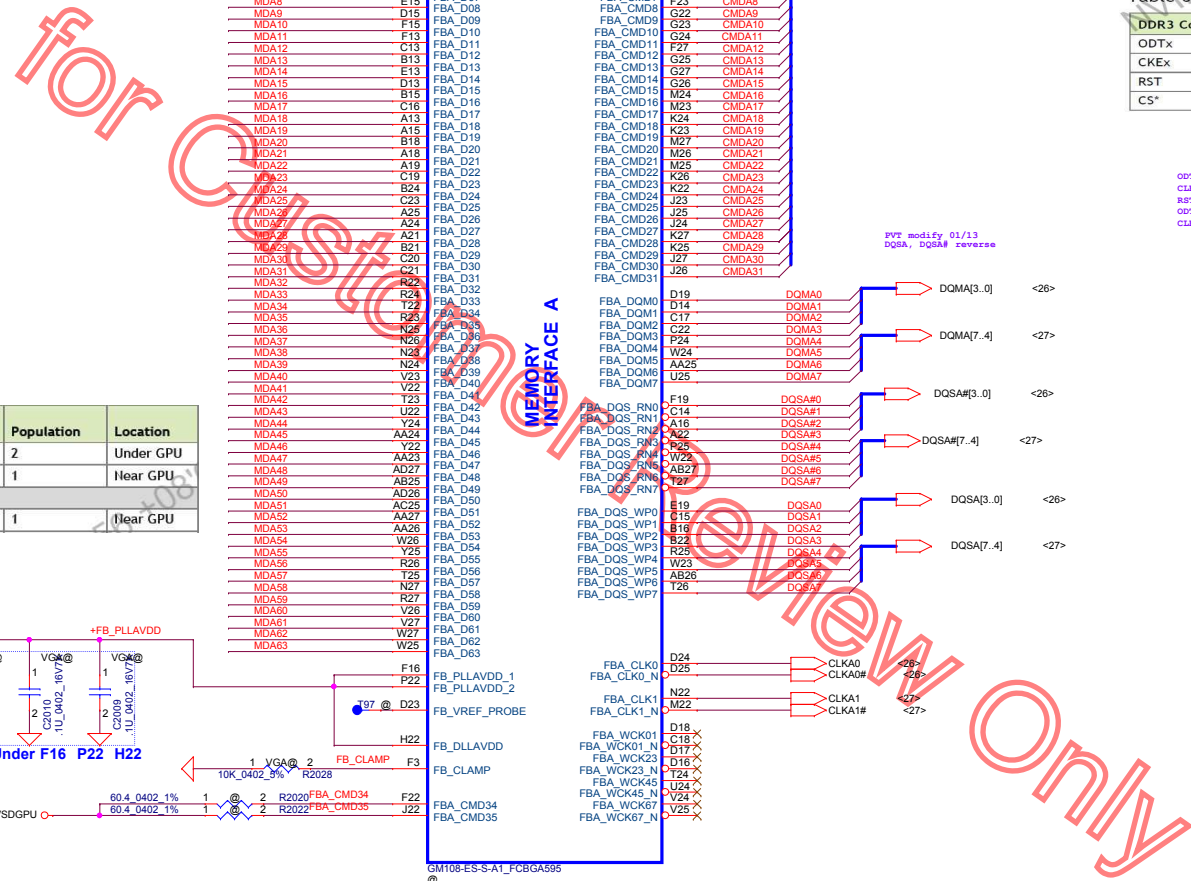
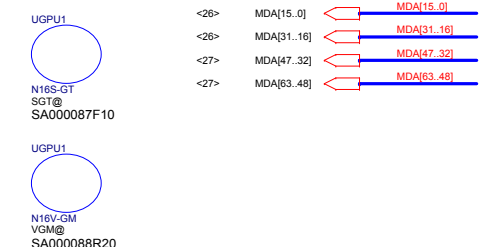
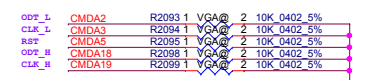


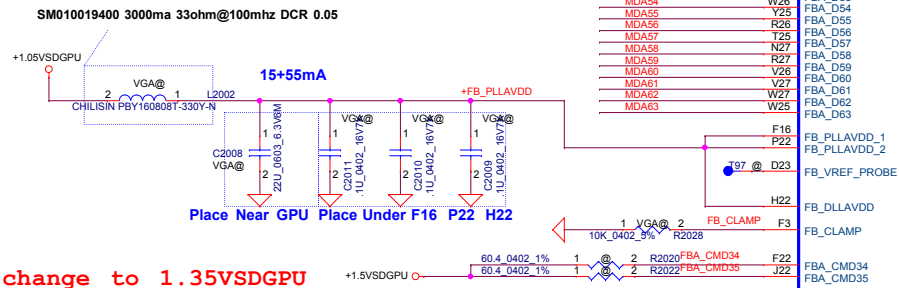
Table 6-8. Memory ODTx, CKEx, and RST Termination

DDR3 Command Bit	Default Pull-Down
ODTx	10 kΩ
CKEx	10 kΩ
RST	10 kΩ
CS*	No Termination



NV 15x DG-06803-V03

GPU Package	Rail	Capacitor Type		Footprint	Population	Location
GB2B-64	FBx_PLL_AVDD and FB_DLL_AVDD Combined	0.1 μF	X7R	0402	2	Under GPU
		22 μF	X5R	0805	1	Near GPU
		Bead Type				
		30 Ω (ESR=0.010 Ω)		0603	1	Near GPU



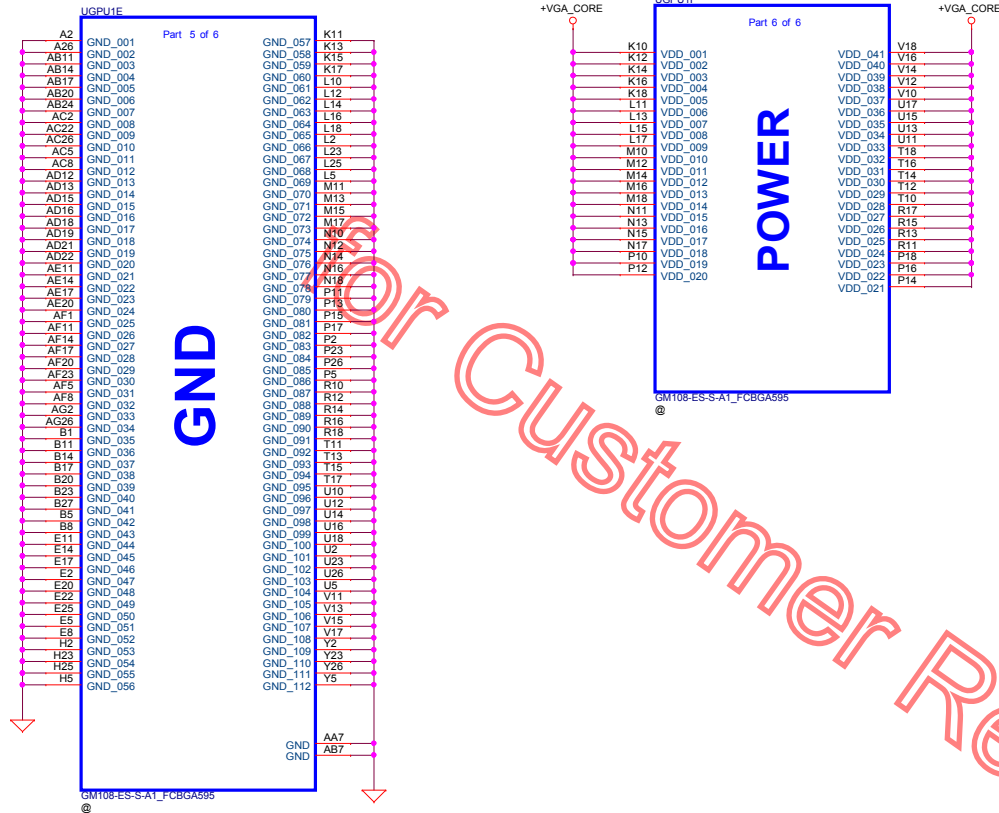
GPU Package Type	Capacitor Type		Footprint		Population	Location
GB2B-64 DDR3	0.1 μ F	X7R	0402	2	2	Under GPU
	1 μ F	X7R	0603	2	2	Under GPU
	4.7 μ F	X6S	0603	2	2	Under GPU
	10 μ F	X5R	0805	1	1	Near GPU
	22 μ F	X5R	0805	1	1	Near GPU

GPU Package Type	Capacitor Type		Footprint	Population	Location
GB2B-64	1.0 μ F	X6S	0402	1	Under GPU
	4.7 μ F	X6S	0603	1	Near GPU
	10 μ F	X5R	0805	1	Midway between GPU and Power Supply
	22 μ F	X5R	0805	1	Midway between GPU and Power Supply

GPU Package	Rail	Capacitor Type	Footprint	Population	Location	
GB2B-64	3V3_MAIN	0.1 μ F	X6S 0402	2	2	Under GPU
GB4B-128		1 μ F	X5R 0603	1	1	Near GPU
GB3-256		4.7 μ F	X5R 0603	1	1	Near GPU
GB2B-64	3V3_AON	0.1 μ F	X6S 0402	1	1	Under GPU
GB4B-128		1 μ F	X5R 0603	1	1	Near GPU
GB3-256		4.7 μ F	X5R 0603	1	1	Near GPU

Capacitor Type	Footprint	Population	Location	
0.1 μ F	X5R	0402	1	Near GPU
4.7 μ F	X5R	0603	2	Near GPU

Capacitor Type		Footprint	Population	Location
0.1 μ F	X6S	0402	1	Under GPU
1.0 μ F	X5R	0603	1	Near GPU
4.7 μ F	X5R	0805	1	Near GPU



NV 15x DG-06803-V03

GPU Package Type	Capacitor Type	Footprint	Population	Location	Comments
GB2B-64	4.7 μ F	X6S	0603	10	10
	1 μ F	X6S	0402	4	4
	47 μ F	X5R	0805	1	1
	22 μ F	X5R	0805	1	1
	4.7 μ F	X5R	0805	5	5
	330 μ F	POS	7343	1	1

DA-06840-V03

Table 6. EDP-Peak

Products	VRM Type	GPU Core	FB Total	1.05V Total
		(A)	(A)	(A)
N15S-GM	DDR3/L	48.11	4.23	0.91
N15S-GT	DDR3/L	60.07	4.26	0.91

DA-06925-V05

Table 6. EDP-Peak at $T_J = 102^\circ\text{C}$

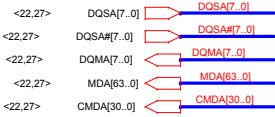
Power Supply Rail	N15V-GM-S
	DDR3/L
(V)	(A)
GPU Core Max	51.50
FB Total	4.25
PEXVDD	2.29

DA07075-V01

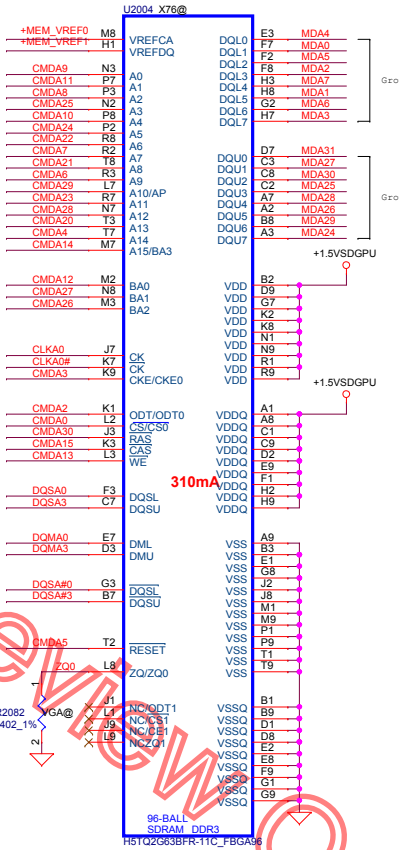
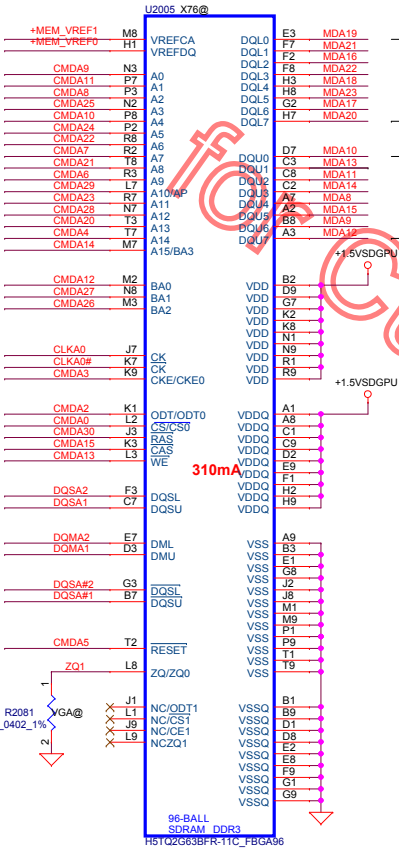
Table 7. EDP-Peak at $T_J = 102^\circ\text{C}$

Power Supply Rail	N15V-GL
	DDR3
(V)	(A)
GPU Core Max	28.26
FB Total	4.07
PEXVDD	1.82

VRAM DDR3 chips



LOW BIT

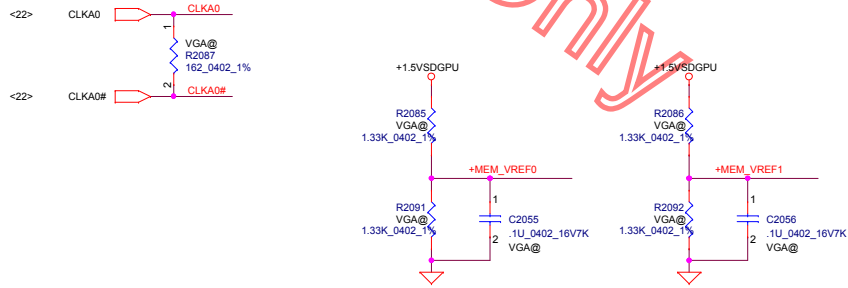
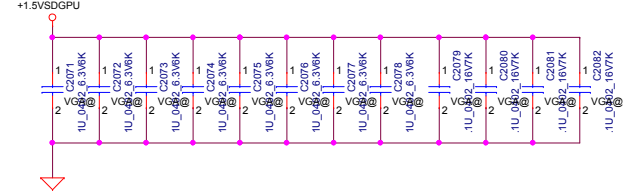


Mode D Address	0..31	32..63
CMD0	CS0_L#	
CMD1		
CMD2	ODT_L	
CMD3	CKE_L	
CMD4	A14	A14
CMD5	RST	RST
CMD6	A9	A9
CMD7	A7	A7
CMD8	A2	A2
CMD9	A0	A0
CMD10	A4	A4
CMD11	A1	A1
CMD12	BA0	BA0
CMD13	WE*	WE*
CMD14	A15	A15
CMD15	CAS*	CAS*
CMD16		CS0_H#
CMD17		
CMD18		ODT_H
CMD19		CKE_H
CMD20	A13	A13
CMD21	A8	A8
CMD22	A6	A6
CMD23	A11	A11
CMD24	A5	A5
CMD25	A3	A3
CMD26	BA2	BA2
CMD27	BA1	BA1
CMD28	A12	A12
CMD29	A10	A10
CMD30	RAS*	RAS*

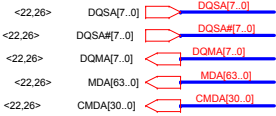
LOW HIGH

Table 3-11. DDR3 per Memory FBVDD/Q Decoupling

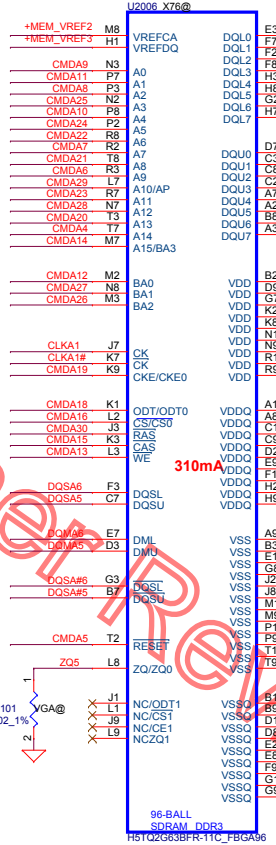
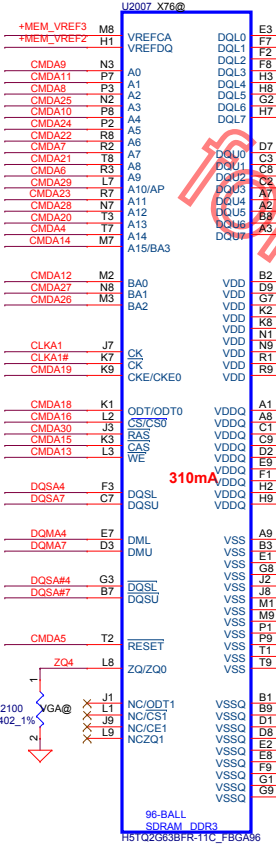
Capacitor Type		Population		Location
FBVDD/Q Combined		FBVDDQ	FBVDD	
0.1 µF	X7R	0402	2	Under DRAM
1.0 µF	X7R	0603	4	Under DRAM
10 µF	X5R	0805	0	Close to DRAM



VRAM DDR3 chips



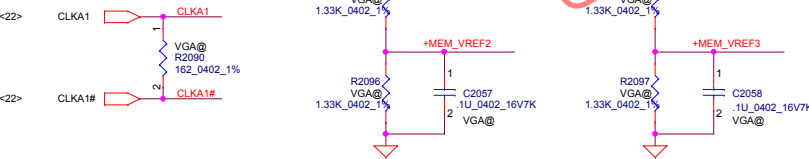
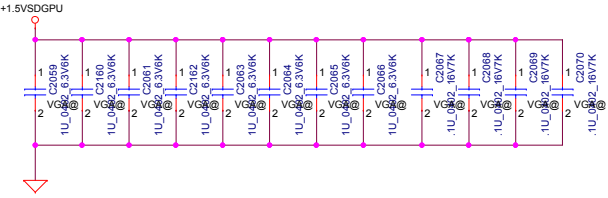
HIGH BIT

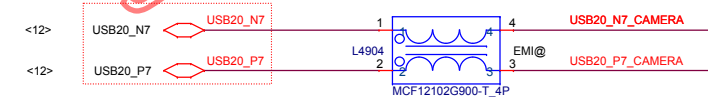
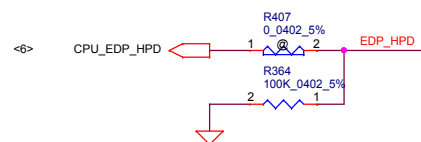
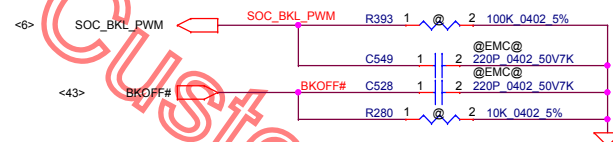
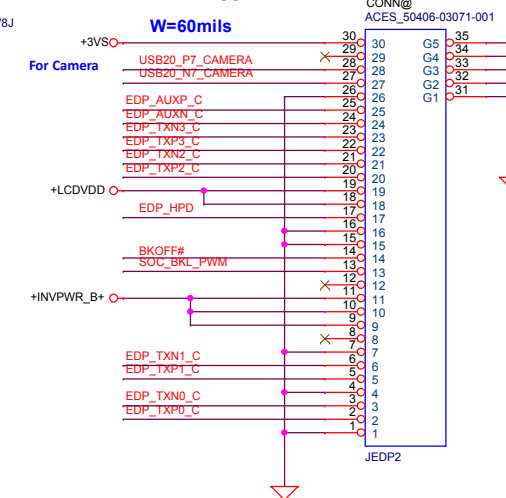
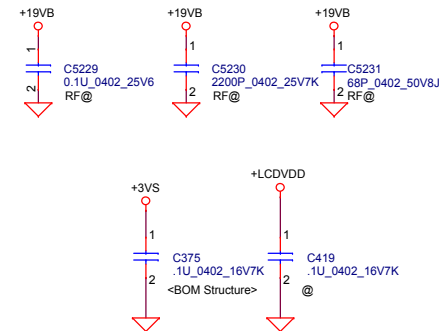
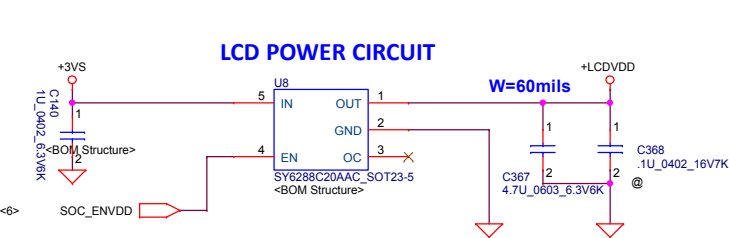


Mode D Address	0..31	32..63
CMD0	CS0_L#	
CMD1		
CMD2	ODT_L	
CMD3	CKE_L	
CMD4	A14	A14
CMD5	RST	RST
CMD6	A9	A9
CMD7	A7	A7
CMD8	A2	A2
CMD9	A0	A0
CMD10	A4	A4
CMD11	A1	A1
CMD12	BA0	BA0
CMD13	WE*	WE*
CMD14	A15	A15
CMD15	CAS*	CAS*
CMD16		CS0_H#
CMD17		
CMD18		ODT_H
CMD19		CKE_H
CMD20	A13	A13
CMD21	A8	A8
CMD22	A6	A6
CMD23	A11	A11
CMD24	A5	A5
CMD25	A3	A3
CMD26	BA2	BA2
CMD27	BA1	BA1
CMD28	A12	A12
CMD29	A10	A10
CMD30	RAS*	RAS*
Not Available		

LOW HIGH

Command Bit	Default Pull-down
ODT*	10k
CKE*	10k
RST	10k
CS*	No Termination

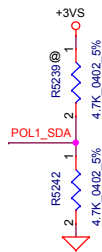
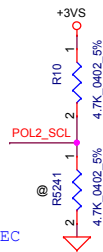




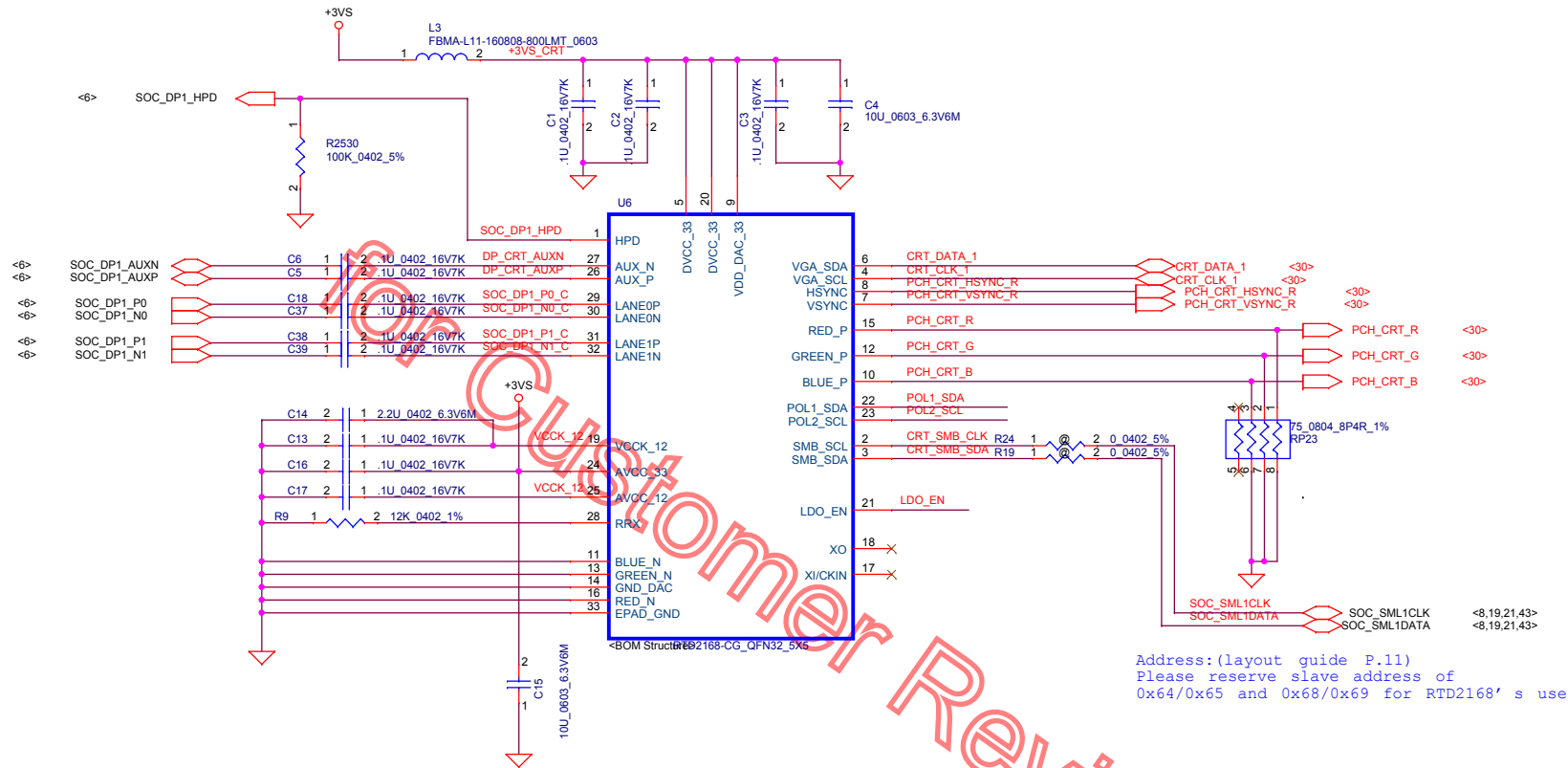
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					Date:	Thursday, December 17, 2015	Sheet

			POL_SDA
		0	1
POL_SCL	0	X	EP
	1	*ROM	EEPROM

ROM: Internal ROM
EP: Programmed external EC
EEPROM: External ROM



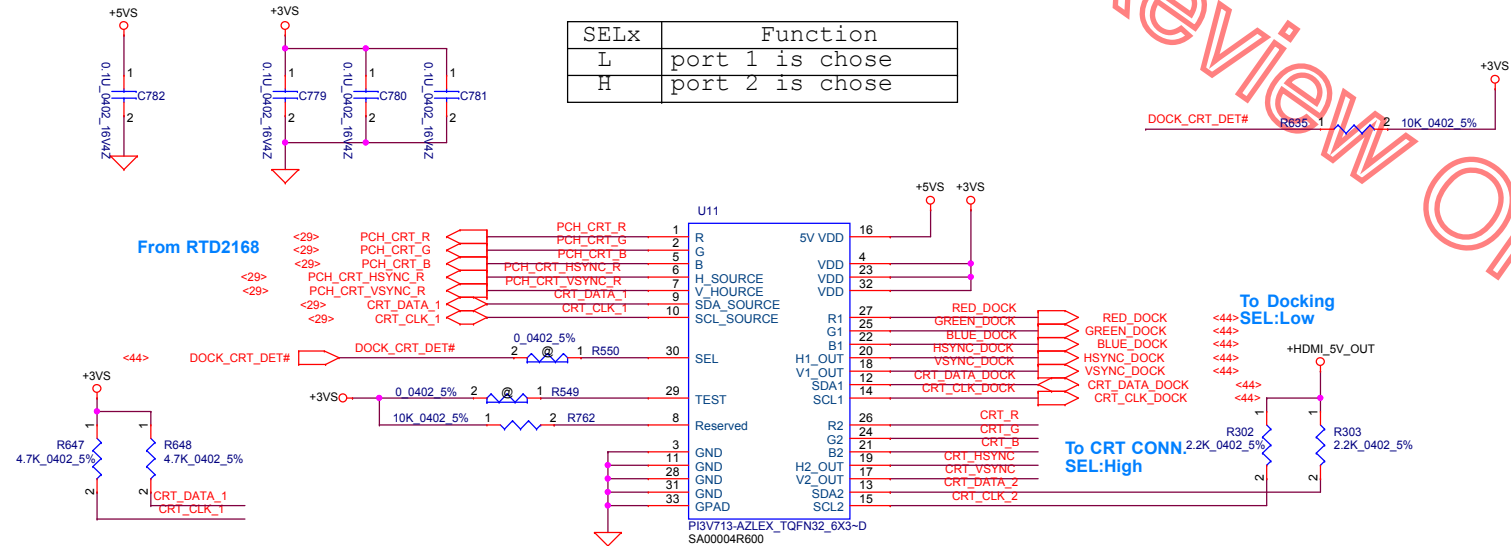
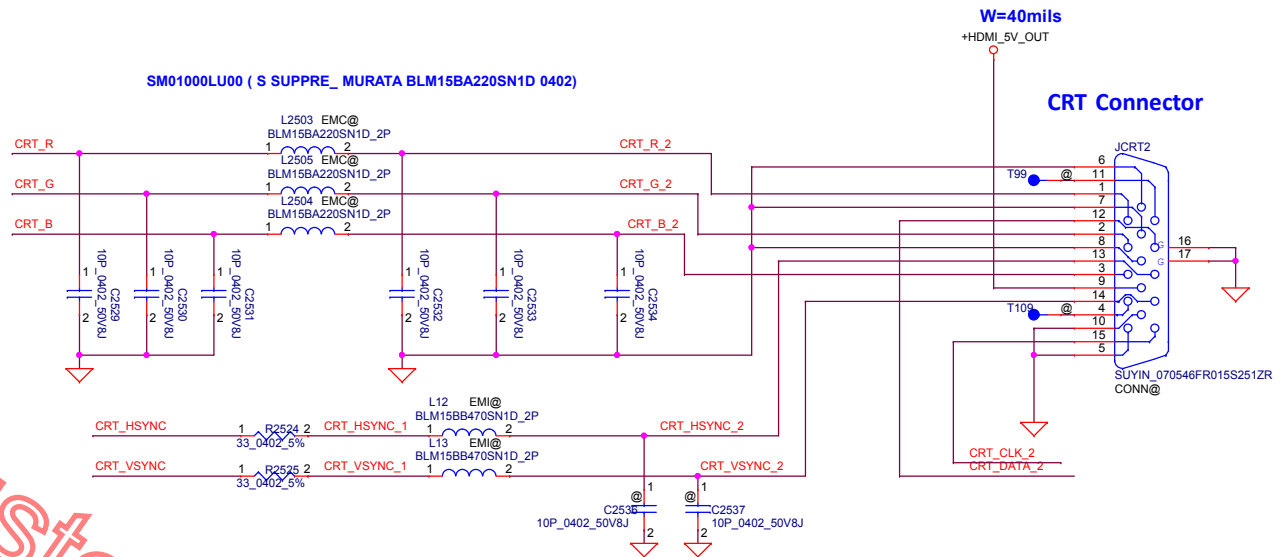
LDO_EN:
*1: Internal 1.2V
0: External 1.2V



Address:(layout guide P.11)
Please reserve slave address of
0x64/0x65 and 0x68/0x69 for RTD2168' s use

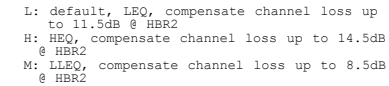
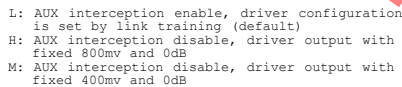
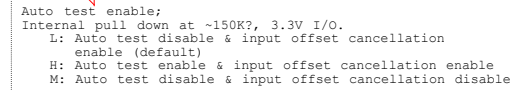
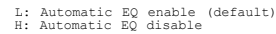
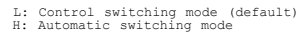
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				Realtek RTD2168	
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				Date: Thursday, December 17, 2015	Rev 0.2
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CRT conn.

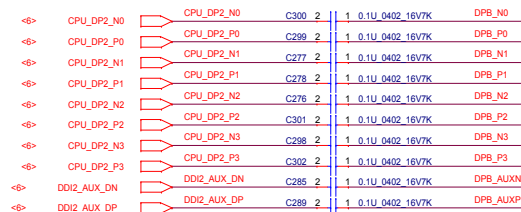


SELx	Function
L	port 1 is chose
H	port 2 is chose

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Issued Date	2014/02/14	Deciphered Date	2015/02/14	CRT CONN.			
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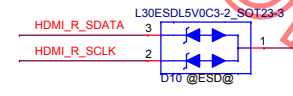
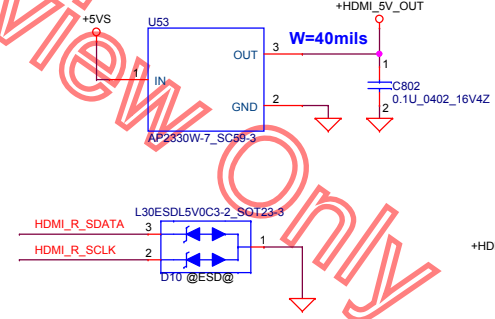
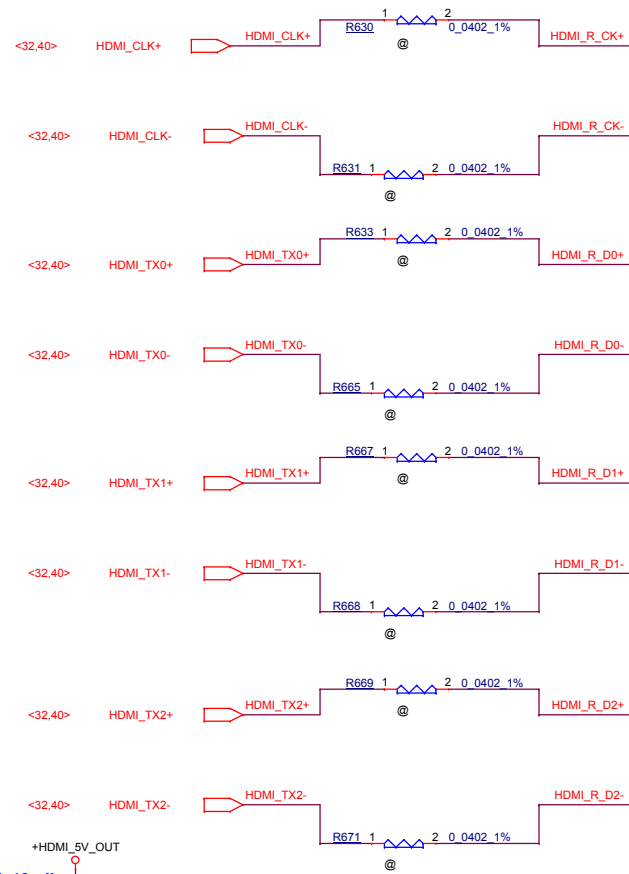
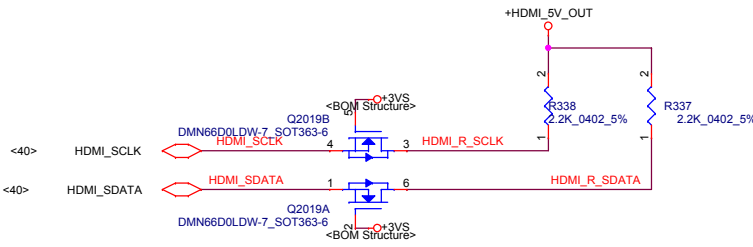
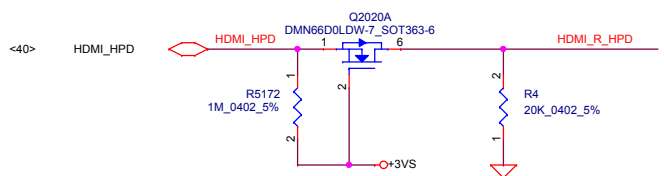
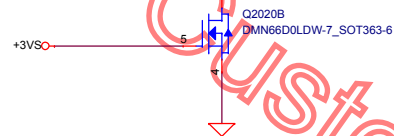
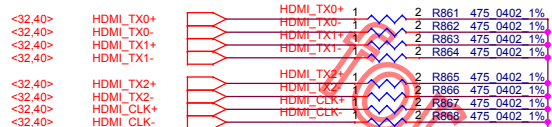


```
Port switching control or priority configuration;
Internal pull down at ~150K $\Omega$ , 3.3V I/O.
  L: Port1 is selected or with higher priority
    (default)
  H: Port2 is selected or with higher priority
```

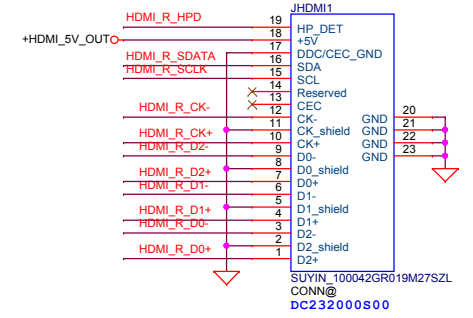


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				P32-DP MUX			
				Size	Document Number	Rev	
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the original BOM structure of R630, R631, R633, R665, R667, R668, R669, R671 is EMI@ , @ is for short pad only

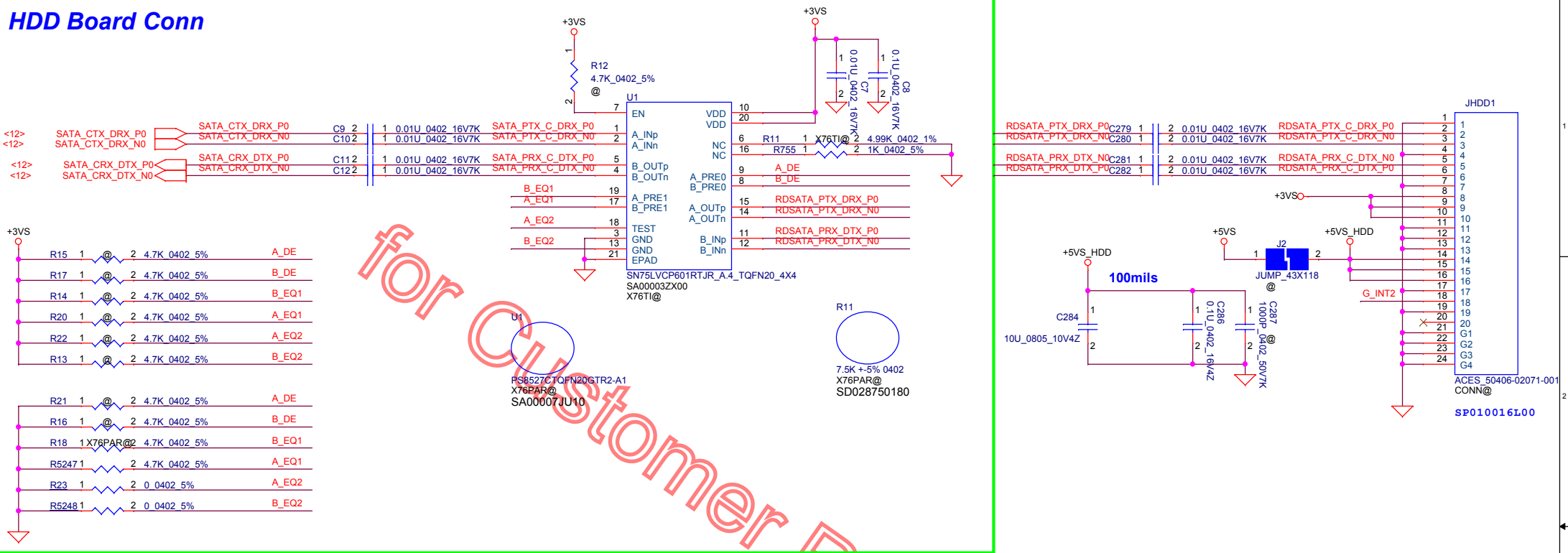


HDMI connector

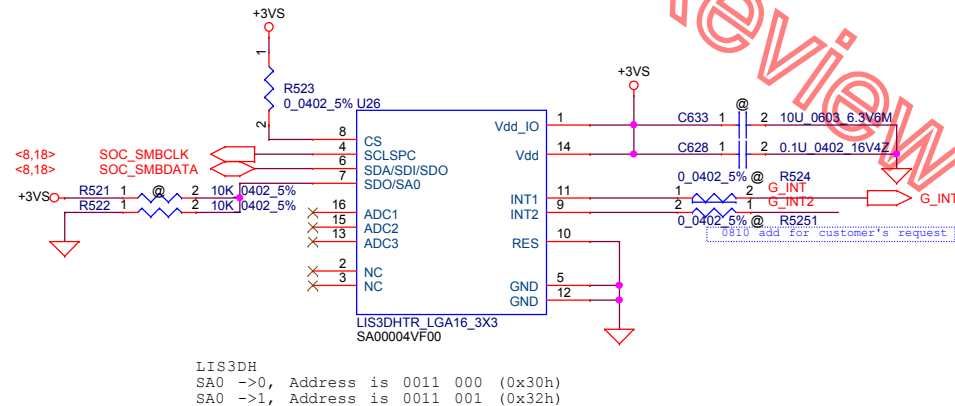


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HDD Board Conn

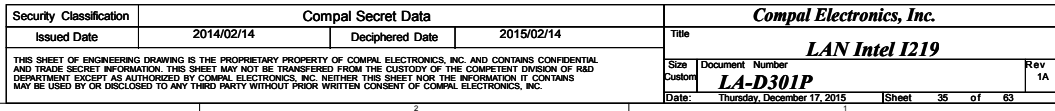


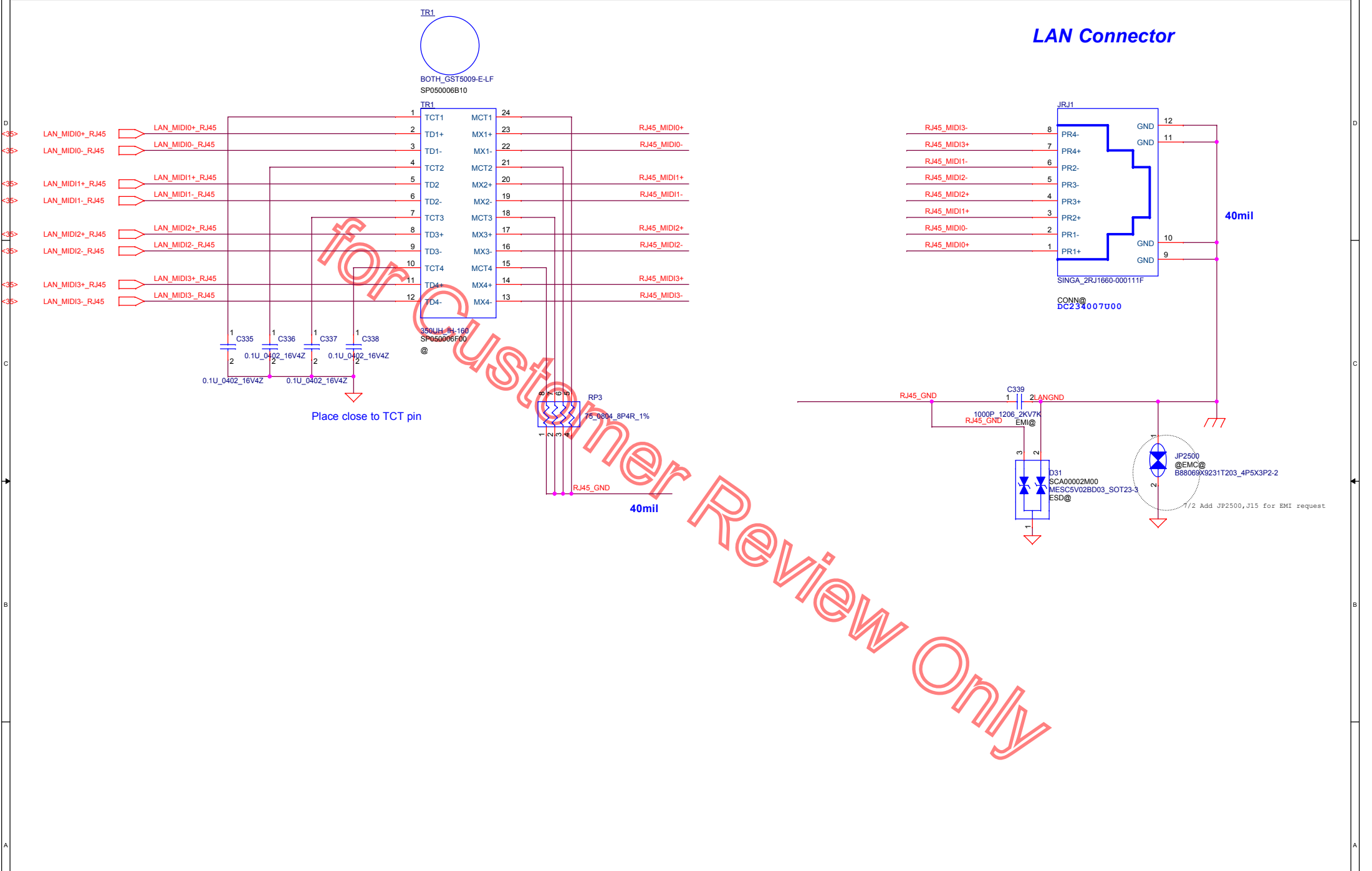
APS G-Sensor



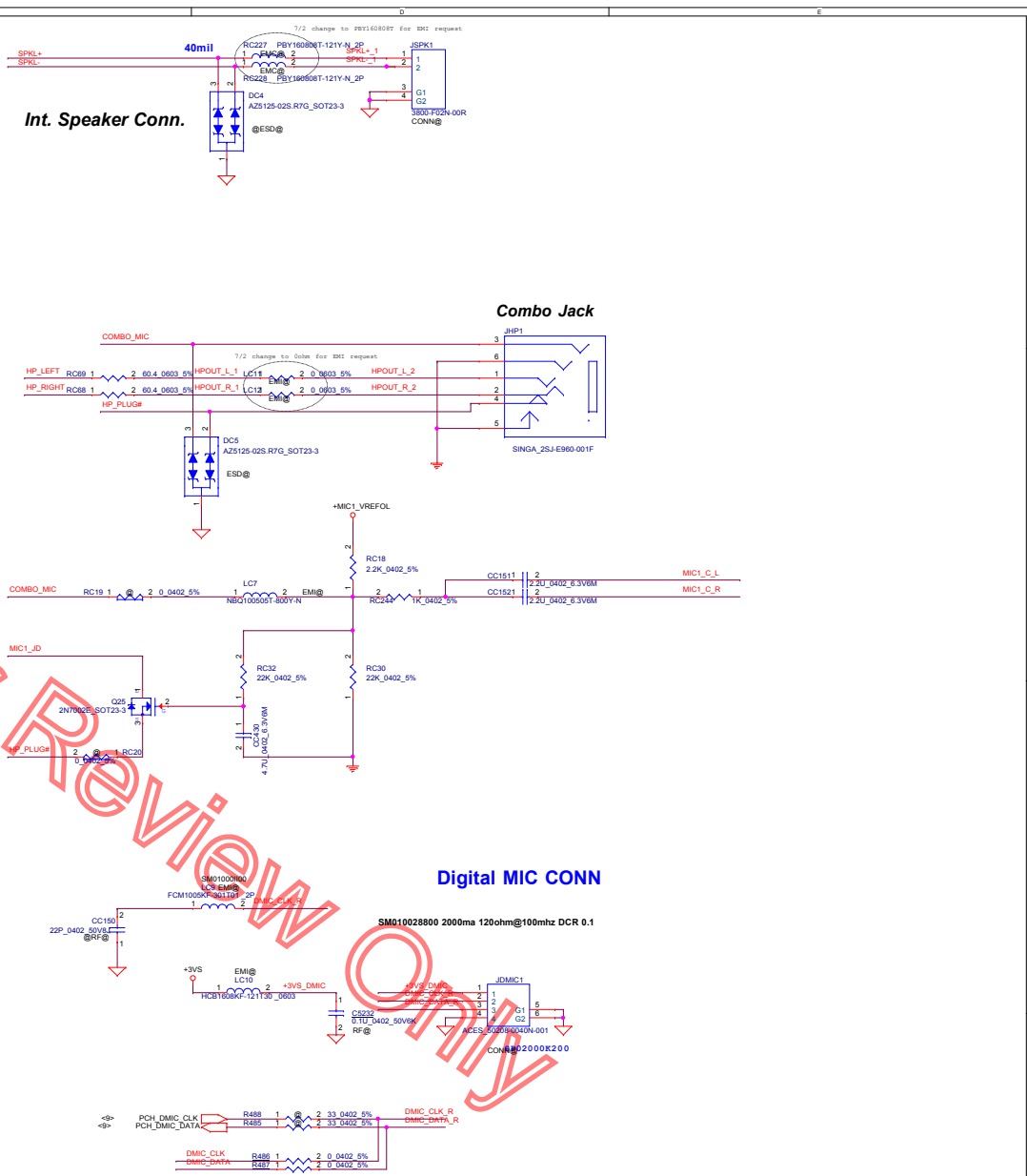
LIS3DH
SA0 ->0, Address is 0011 000 (0x30h)
SA0 ->1, Address is 0011 001 (0x32h)

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Size	Document Number	Rev		1A	
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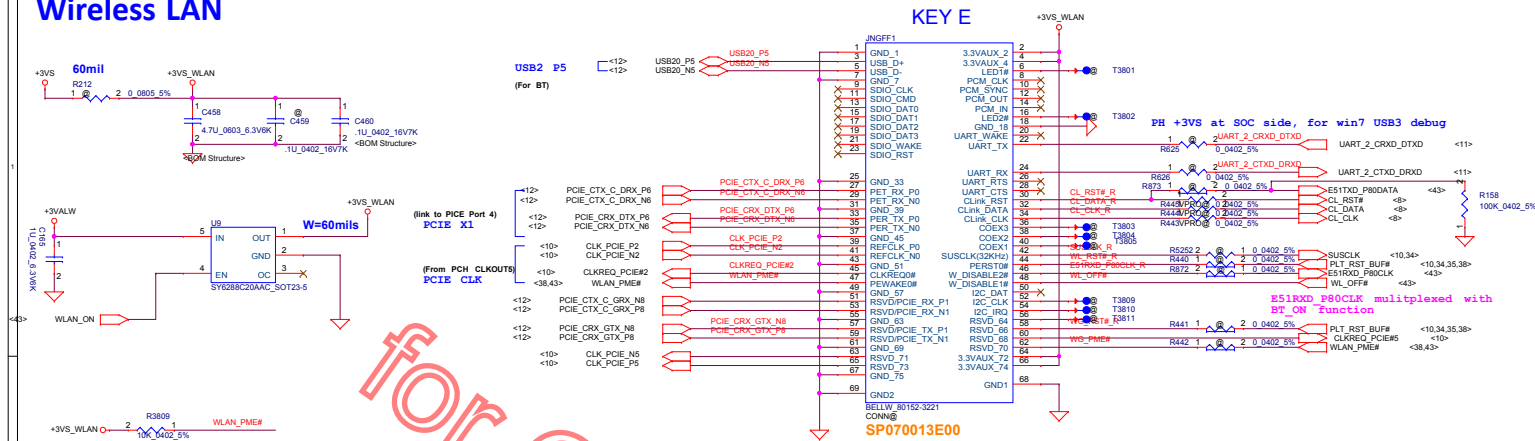


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Wireless LAN



NGFF WL+BT+WIGIG (KEY E)

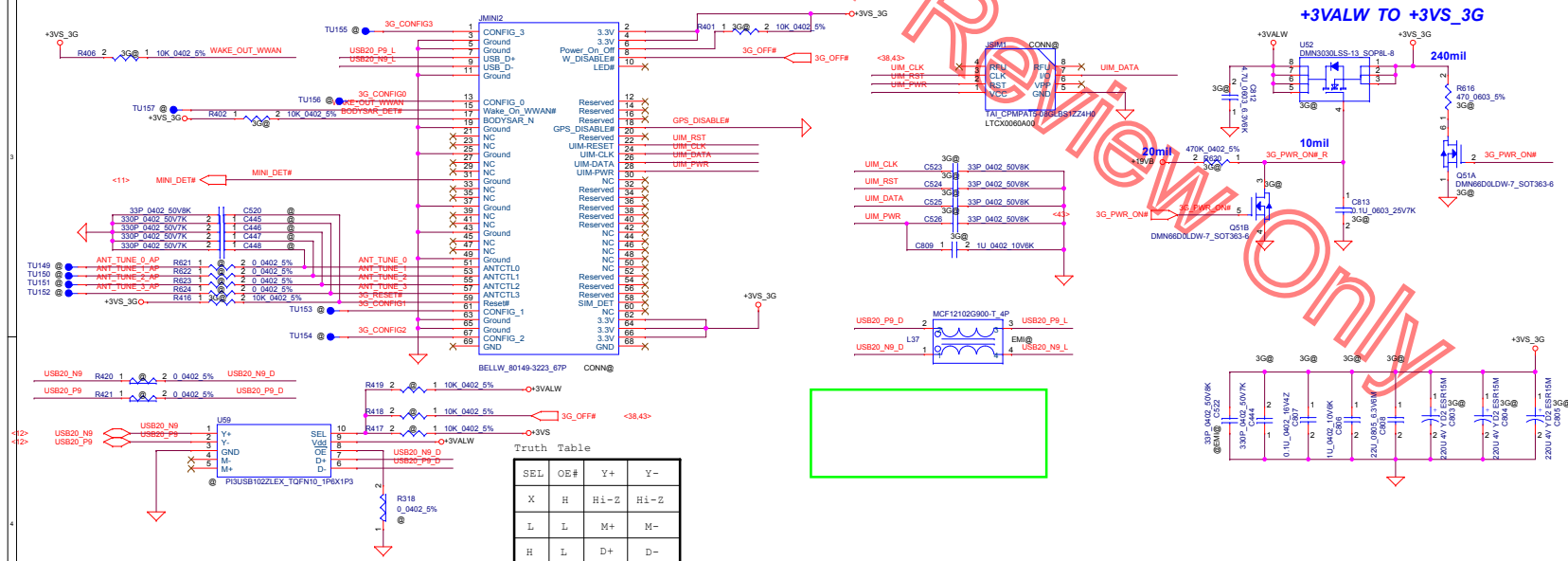
WiGig/WLAN/BT Combo Host Pin Configuration

	M.2			M.2		
	MODE	Pin	Standard Definition	Standard Definition	Pin	MODE
5%	MODE_0/0	74	3.3V	QND	75	NC
	MODE_0/1	72	3.3V	REFCLKIN1	73	10k Ω PULL-UP
	10k Ω PULL-UP			REFCLKIN1	71	10k Ω PULL-UP
	10k Ω PULL-UP	70	PEWAKEUP	QND	69	3.3V
	MODE_0/CLKREQ0	68	CLKREQ0/1	PETM1	67	10k Ω PULL-UP
	MODE_0/PERSTN	66	PERST/1	PETP1	66	10k Ω PULL-UP
	10k Ω PULL-UP			QND	65	3.3V
	10k Ω PULL-UP	64	Reserved	PERP1	64	10k Ω PULL-UP
	10k Ω PULL-UP	62	ALERT#	PERM1	63	10k Ω PULL-UP
	MODE_0/DT0	58	IO-CLK	PERM1	61	10k Ω PULL-UP
	10k Ω PULL-UP			QND	59	3.3V
	MODE_0/DT1	58	IO-DATA	PEWAKEUP	55	10k Ω PULL-UP
	EDGE_0/WDIASBL#	56	WDIASBL#	CLKREQIN0	55	10k Ω PULL-UP
	EDGE_0/WDIASBL#	56	WDIASBL#	QND	54	3.3V
	MODE_0/PERSTN	52	PERST/0	REFCLKIN0	49	10k Ω PULL-UP
	50	SUSCLK2(32MHz)		REFCLKIN0	47	10k Ω PULL-UP
	NC	48	IOCE0	REFCLKIN0	47	10k Ω PULL-UP
	NC	46	IOCE2	QND	45	3.3V
	NC	44	IOCE1	PETM0	44	10k Ω PULL-UP
	10k Ω PULL-UP			PETM0	41	10k Ω PULL-UP
	MODE_0/DPH1**	40	Reserved	QND	39	3.3V
	10k Ω PULL-UP			PERM0	37	10k Ω PULL-UP
	MODE_0/DPH1**	36	NC	PETM0	35	10k Ω PULL-UP
	MODE_0/DPH1**	34	NC	QND	33	3.3V
	MODE_0/DPH1**	32	NC	NOTCH	NOTCH	NOTCH
	NOTCH	NOTCH	NOTCH	NOTCH	NOTCH	NOTCH
	NOTCH	NOTCH	NOTCH	NOTCH	NOTCH	NOTCH
	NOTCH	NOTCH	NOTCH	NOTCH	NOTCH	NOTCH
	MODE_0/TRST	22	NC	NC	23	NC
	MODE_0/NC	20	NC	NC	21	NC
	MODE_0/NC	18	NC	NC	19	NC
	MODE_0/NC	16	NC	NC	17	NC
	EDGE_0/LEDA	15	LEDA	NOTCH	NOTCH	NOTCH
	NOTCH	NOTCH	NOTCH	NOTCH	NOTCH	NOTCH
	NOTCH	NOTCH	NOTCH	QND	7	3.3V
	EDGE_0/LEDB	6	LEDB	USB_D-	5	10k Ω PULL-UP
	MODE_0/0	4	3.3V	USB_D+	3	10k Ω PULL-UP
	MODE_0/0	2	3.3V	QND	1	3.3V

3.1.8.1.3.1.7.1. UART Wakeup

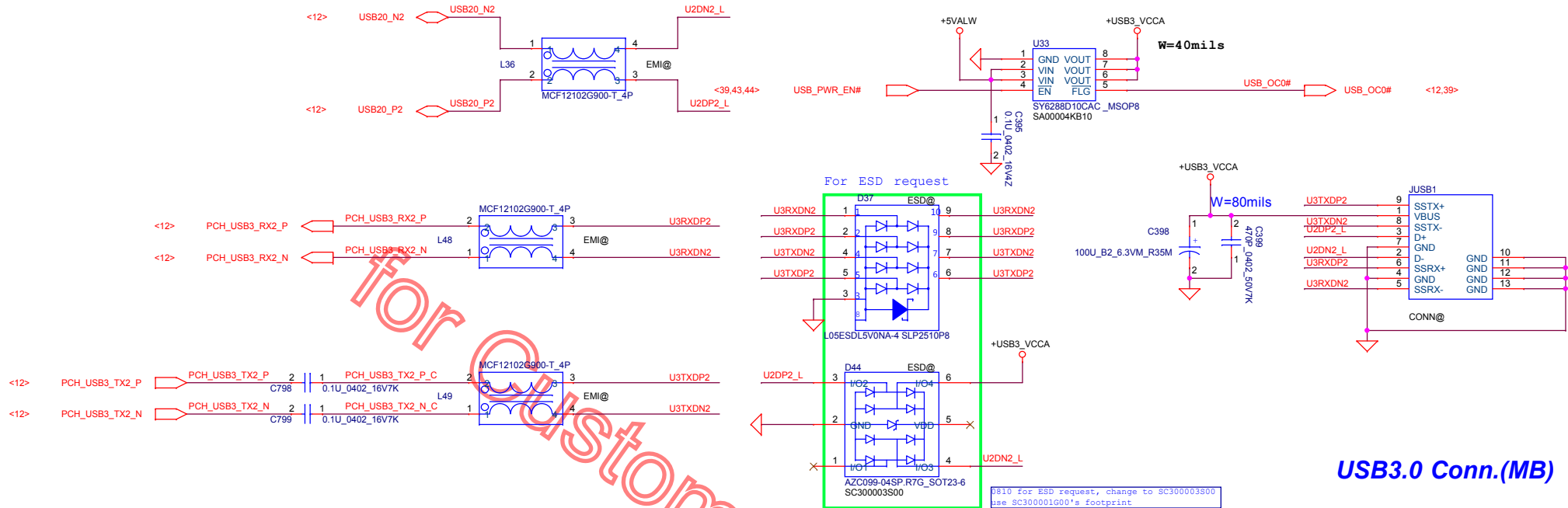
The UART power management protocol supports the following 4-wire and 5-wire interfaces:

- ❑ **RTS** **UART RXD**: (Input): Receive Data
- ❑ **RTS** **UART TXD**: (Output): Transmit Data
- ❑ **UART RTS**: (Input): Request to Send (Host Flow Control)
- ❑ **UART CTS**: (Output): Clear to Send (Device Flow Control)
- ❑ **Host Wake-Up** **UART Wake#**: (Output): Host wake-up line is optional in case the host support in-band wake-up

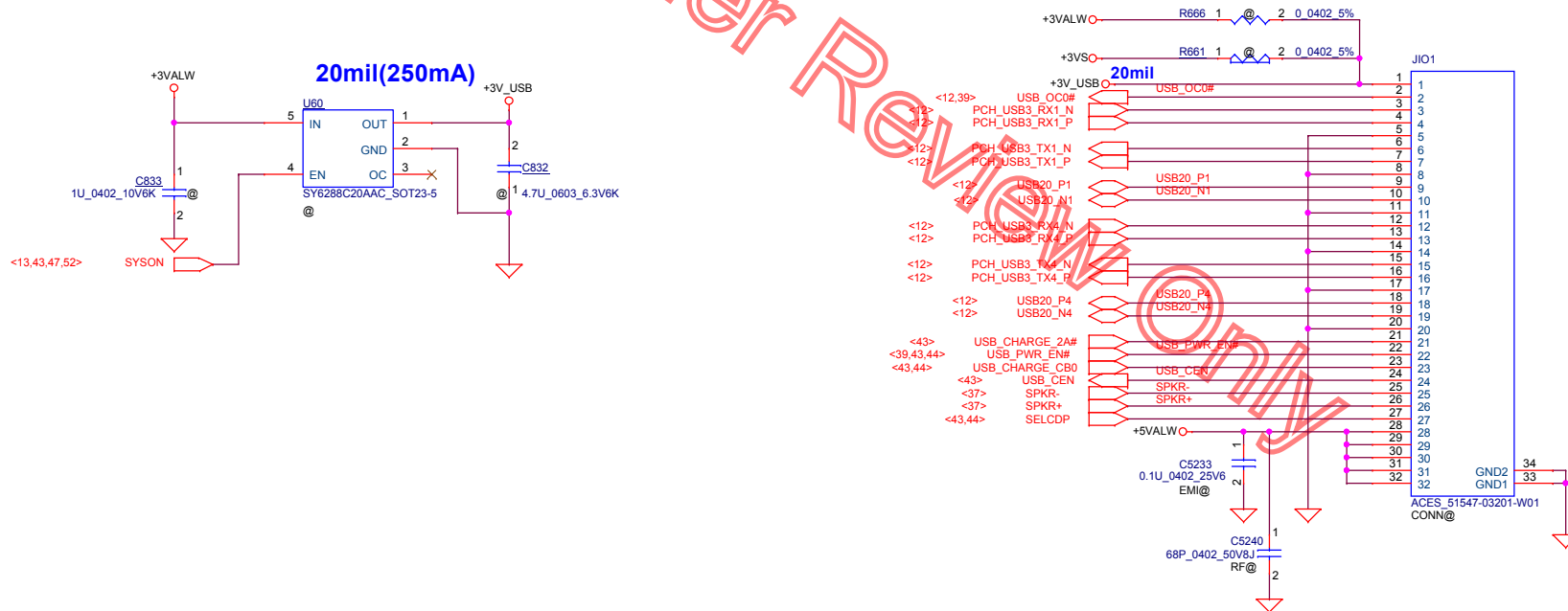


SEL	OE#	Y+	Y-
X	H	Hi-Z	Hi-Z
L	L	M+	M-
H	L	D+	D-

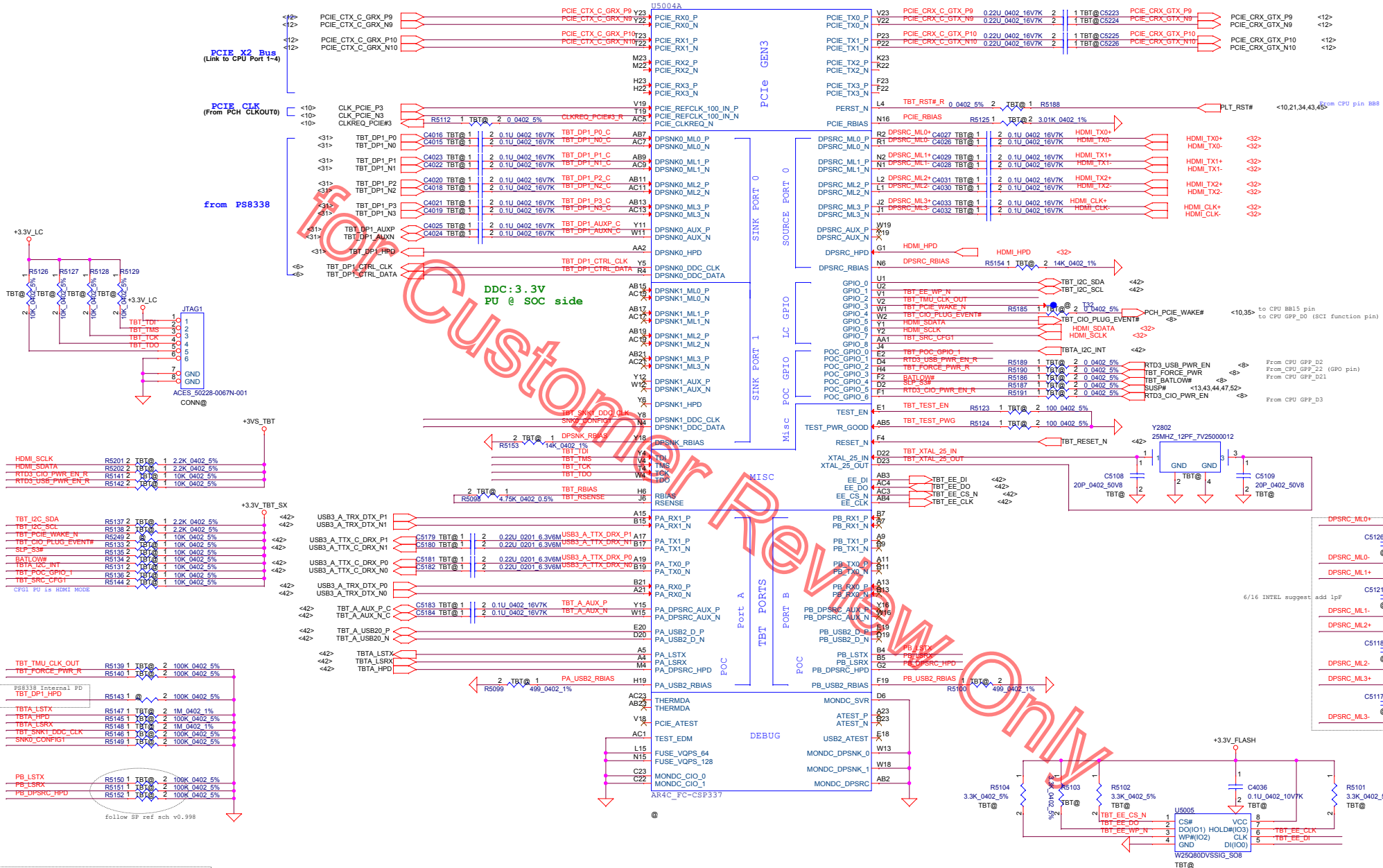
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IO Board Conn(For FFC,FPC)



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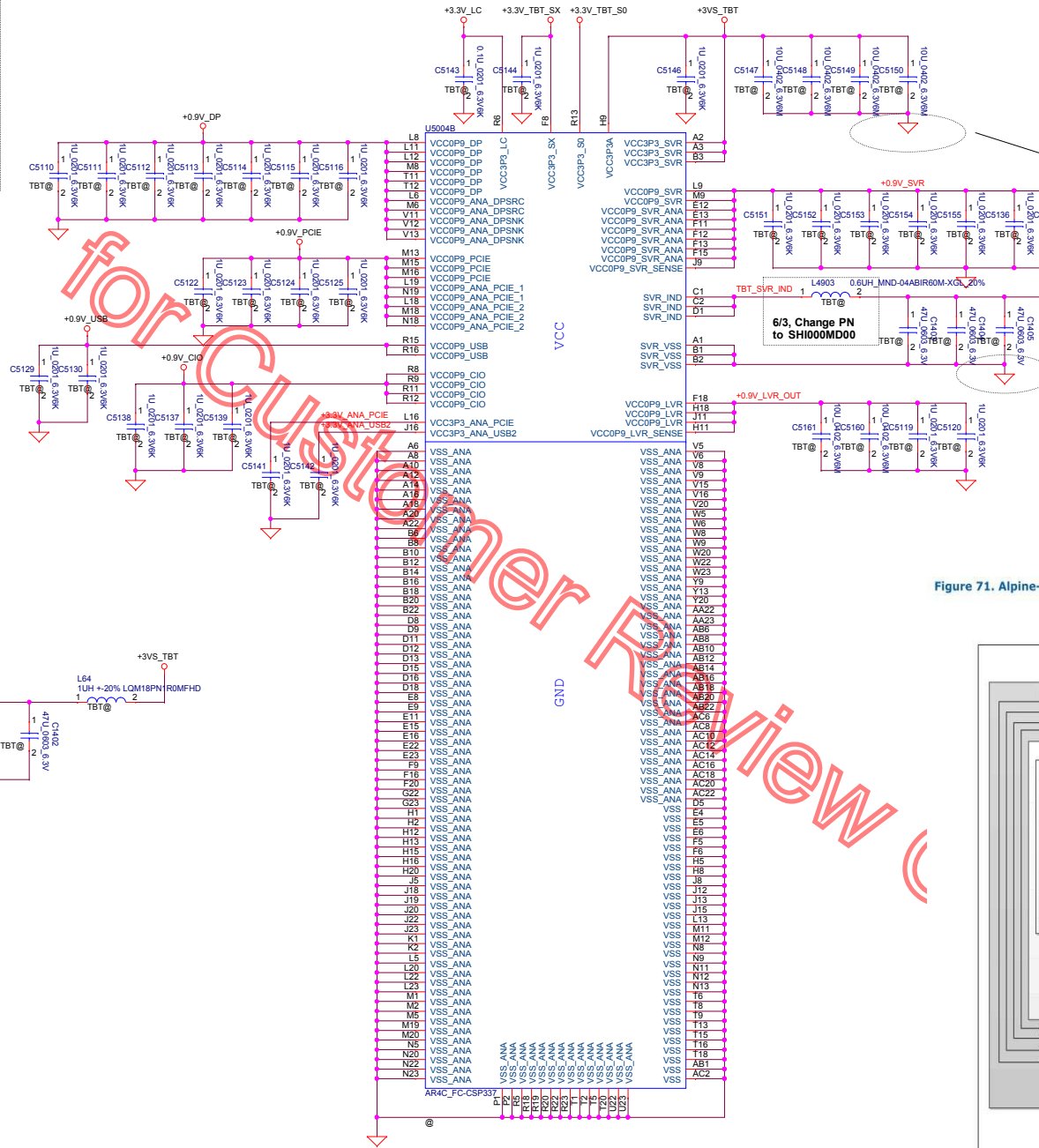
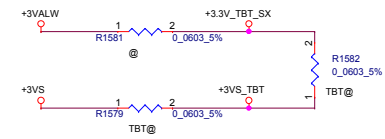
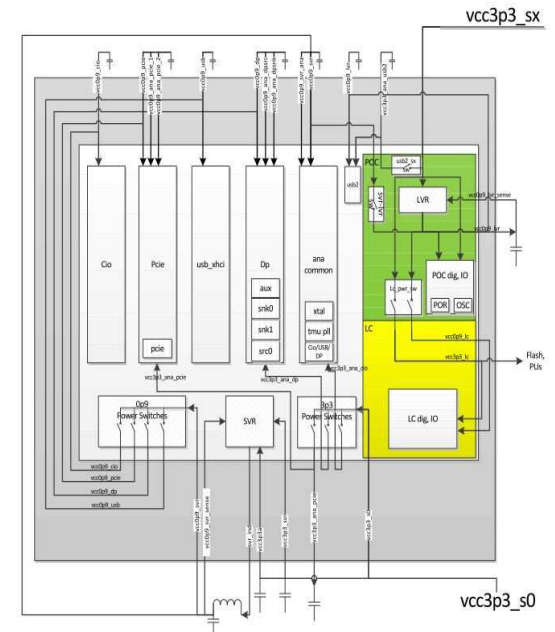
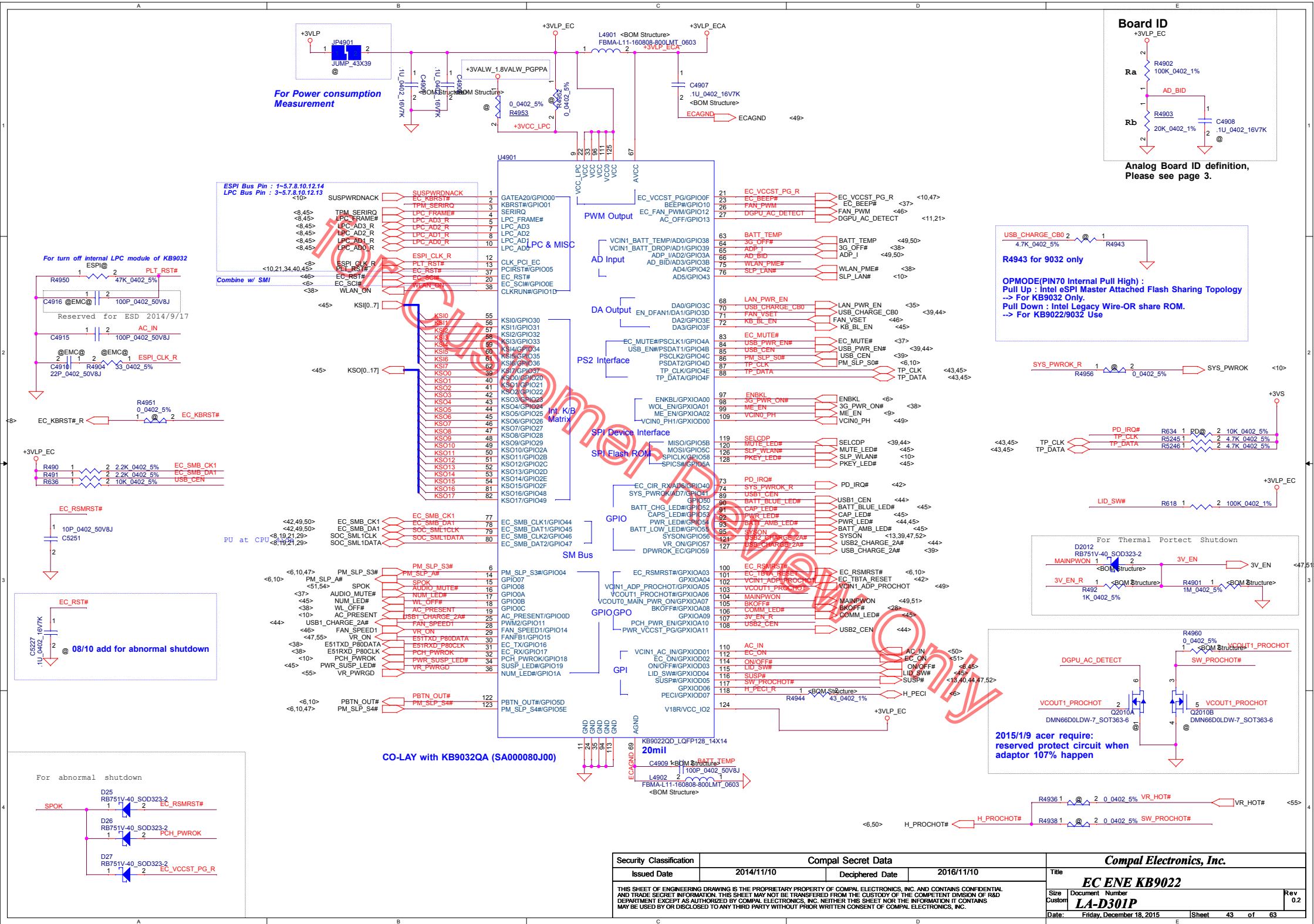


Figure 71. Alpine-Ridge SP Power Delivery



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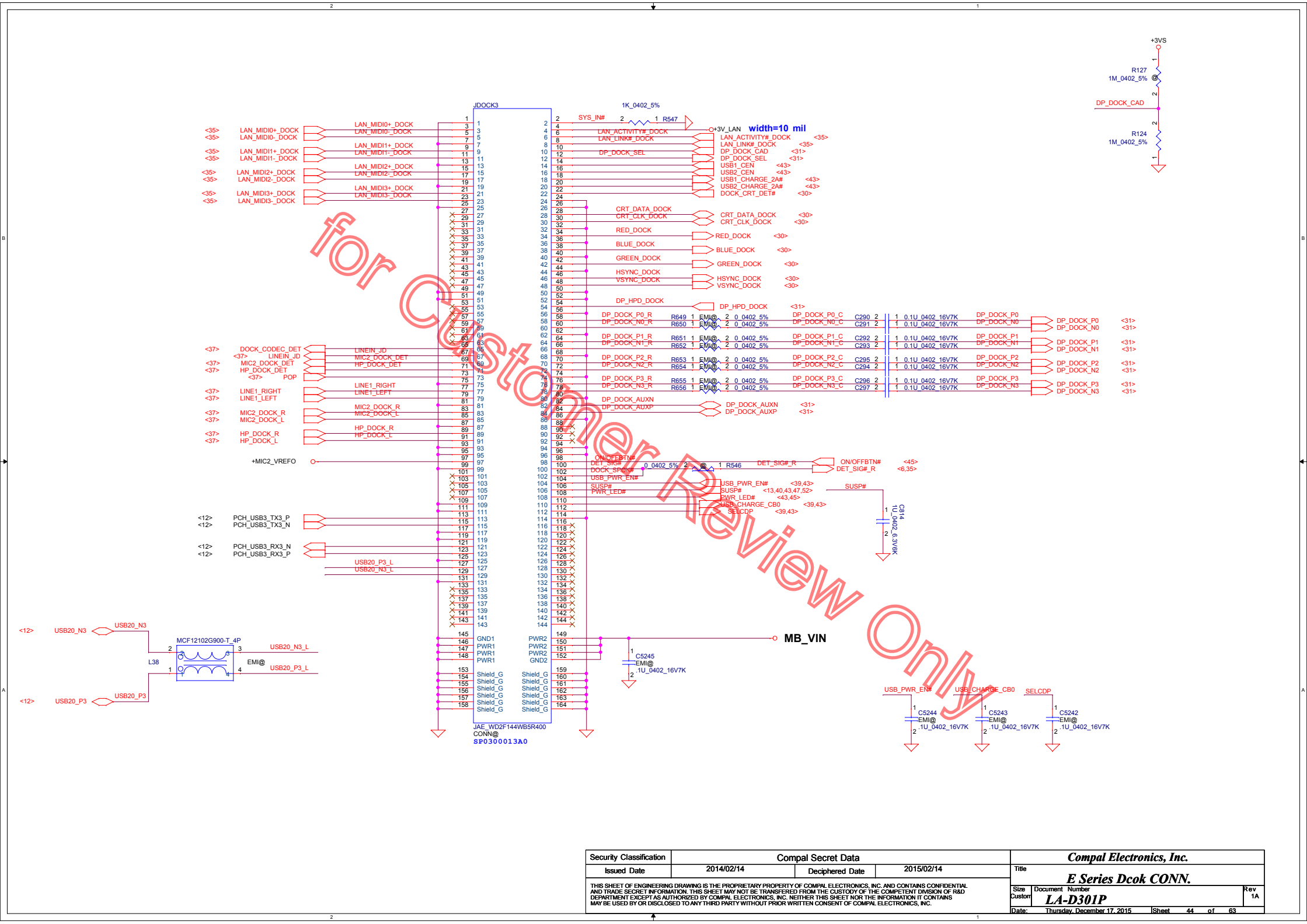


Diagram illustrating the pinout of the ACES 50565-026N-001-26P connector. The diagram shows two rows of pins, each with 13 pins. The top row is labeled KS[0..7] and the bottom row is labeled KS[0..17]. The pins are numbered 1 through 26. The top row pins are labeled KS00 through KS12, and the bottom row pins are labeled KS13 through KS25. The diagram also shows two rows of pins labeled 68P_0402_50V8UJ and RF, with pins 1 and 2 on the left and pins 3 and 4 on the right. A note at the bottom states: "If JVS closed JWS need to place 2 68p CAPs".

Pin	Function
1	68P_0402_50V8UJ
2	RF
3	C5236
4	RF
5	KS[0..7]
6	KS[0..17]
7	KS[0..7]
8	KS[0..17]
9	KS[0..7]
10	KS[0..17]
11	KS[0..7]
12	KS[0..17]
13	KS[0..7]
14	KS[0..17]
15	KS[0..7]
16	KS[0..17]
17	KS[0..7]
18	KS[0..17]
19	KS[0..7]
20	KS[0..17]
21	KS[0..7]
22	KS[0..17]
23	KS[0..7]
24	KS[0..17]
25	KS[0..7]
26	KS[0..17]

ACES 50565-026N-001-26P
CONN#

SFP1001IIE00

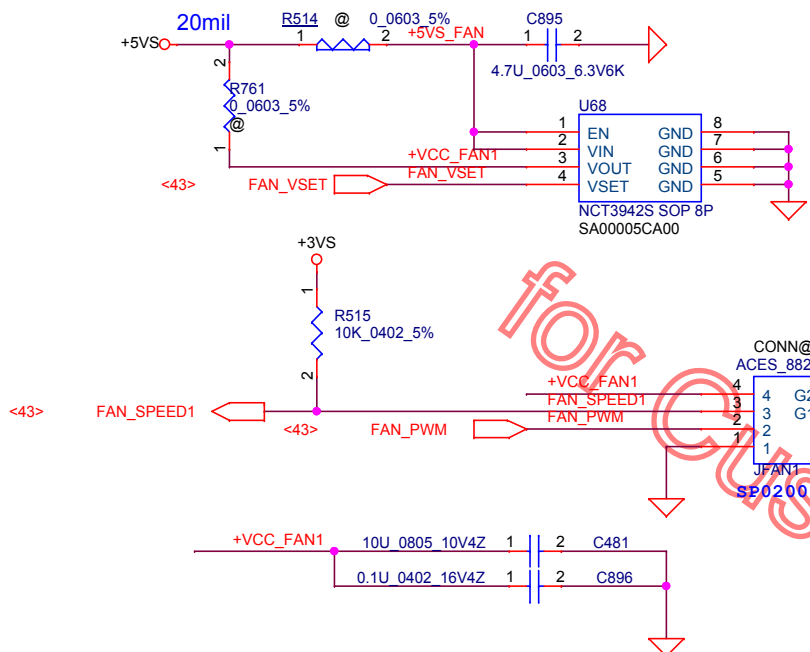
[illegible]

Signal	Pin	Connector Pin
<12> POIE_CTX_C_DRX_P11	1	1
<12> POIE_CTX_C_DRX_N11	2	2
CLK_POIE_CARD	3	3
CLK_POIE_CARD#	4	4
POIE_CRX_DTX_P11	5	5
POIE_CRX_DTX_N11	6	6
CLKREQ_POIE#A	7	7
CLKREQ_POIE#A	8	8
CLKREQ_POIE#A	9	9
CLKREQ_POIE#A	10	10
CLKREQ_POIE#A	11	11
CLKREQ_POIE#A	12	12
CLKREQ_POIE#A	13	13
CLKREQ_POIE#A	14	14
CLKREQ_POIE#A	15	15
CLKREQ_POIE#A	16	16
CLKREQ_POIE#A	17	17
CLKREQ_POIE#A	18	18
CLKREQ_POIE#A	19	19
CLKREQ_POIE#A	20	20

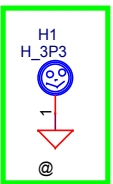
ACES 50505-0164N-001
CONN#

[illegible][illegible]

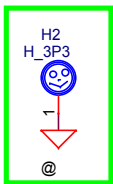
FAN Conn



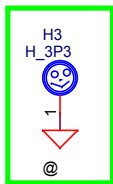
WIFI Stand off



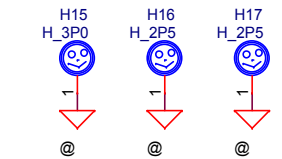
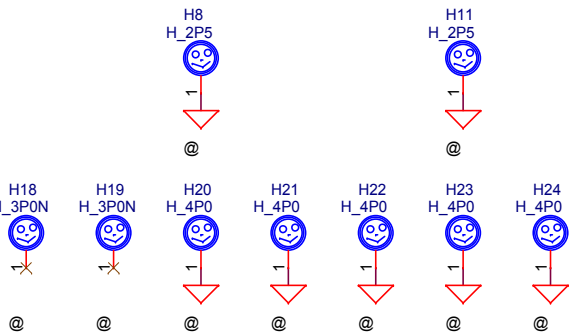
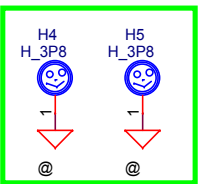
3G Stand off



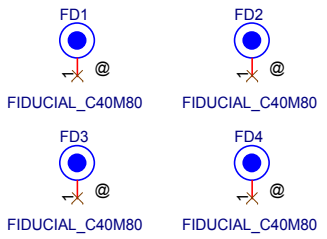
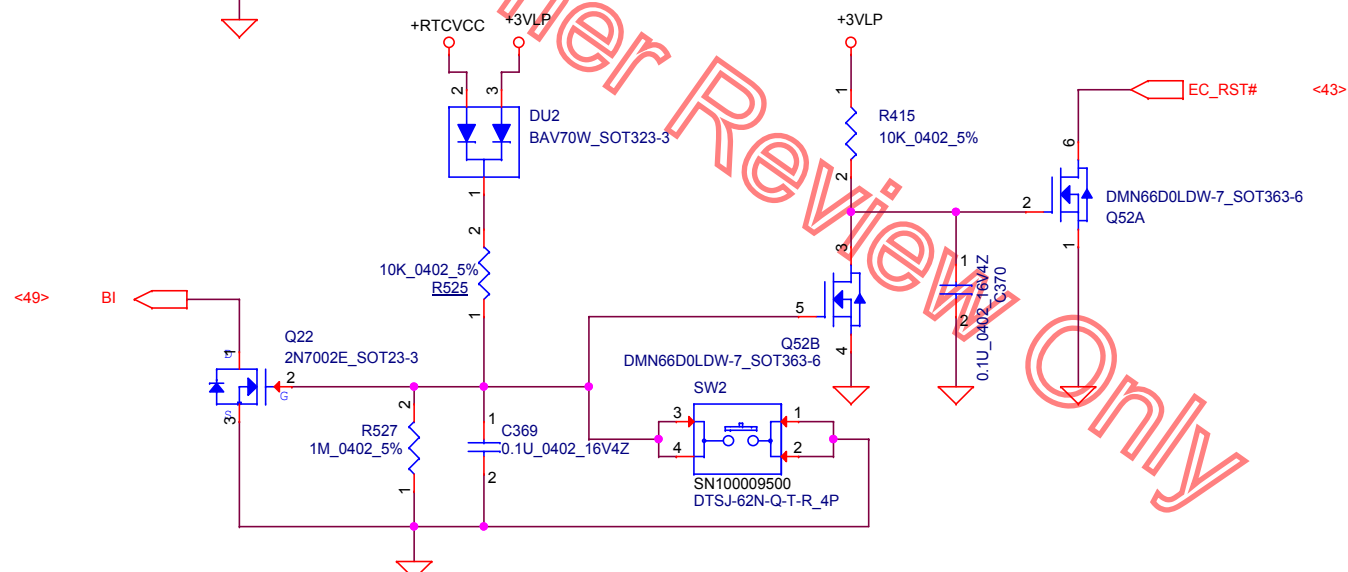
SSD Stand off



FAN Stand off

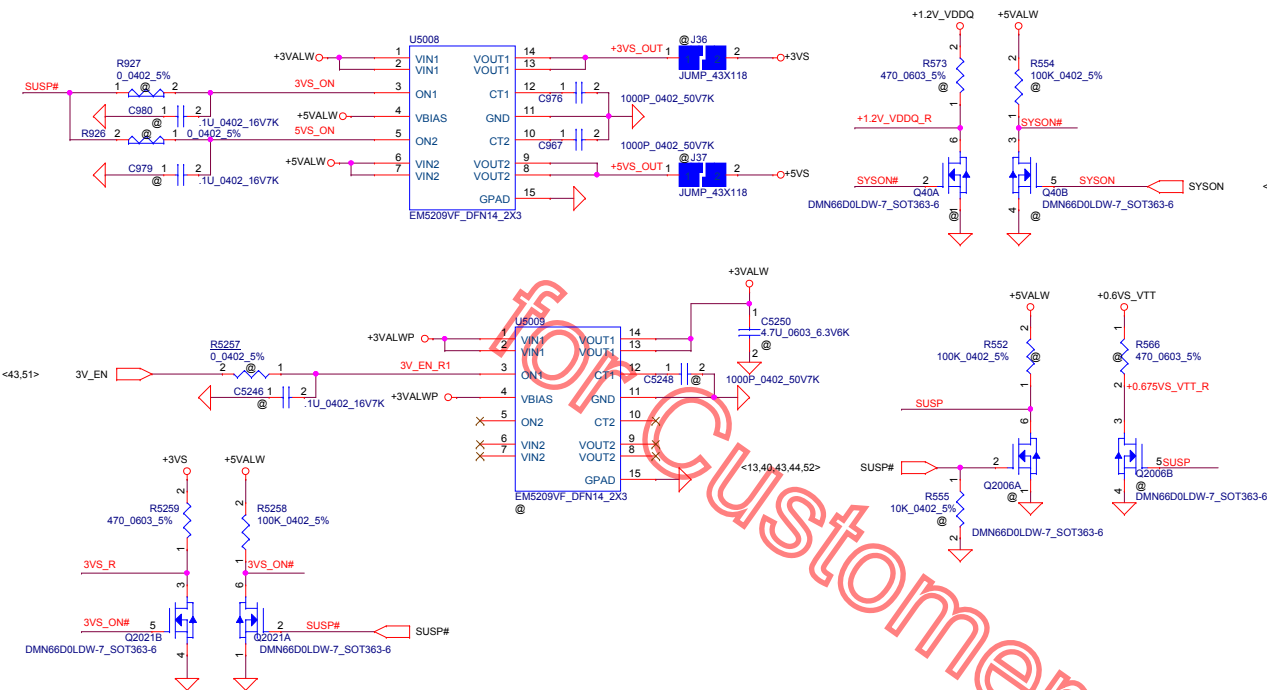


locate MB

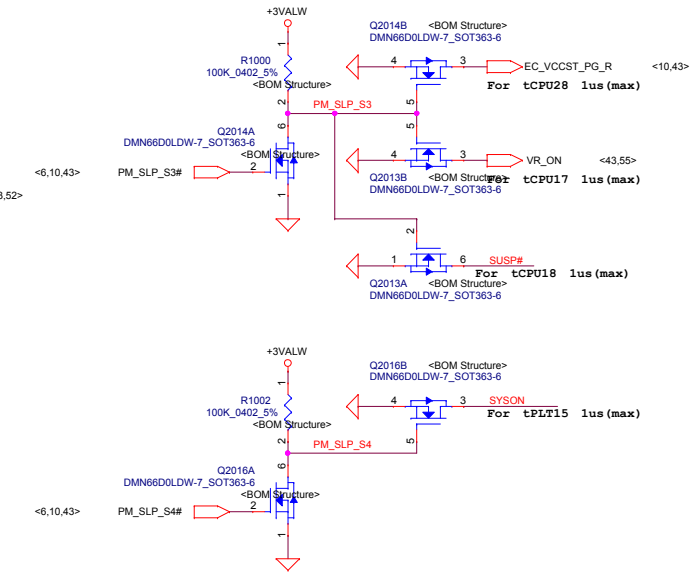


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				Size Custom	Rev 1A
				Document Number	LA-D301P
				Date:	Thursday, December 17, 2015
				Sheet	46 of 63

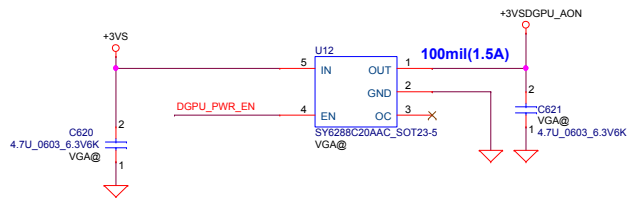
DC & VGA Interface



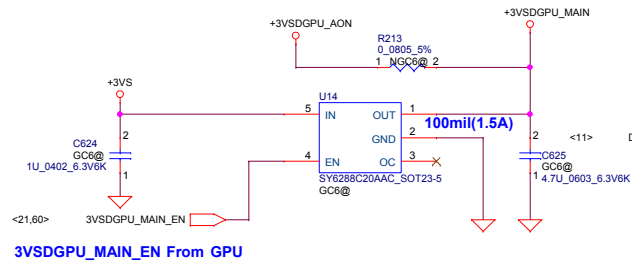
For Power Of f Sequence



+3VS to +3VSDGPU_AON for GPU

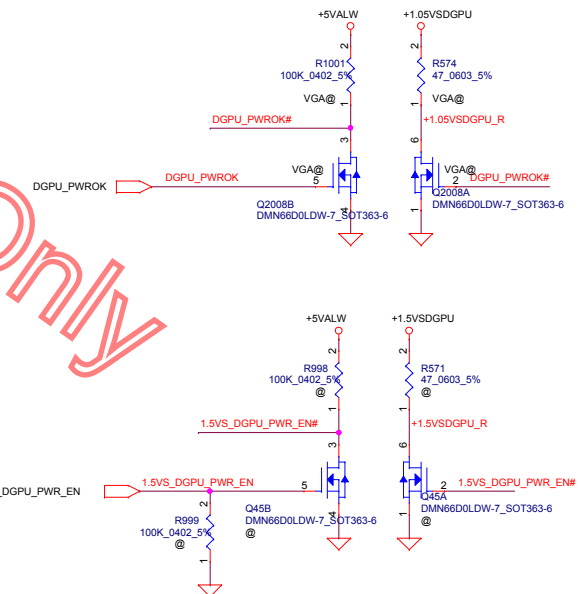
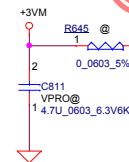


+3VS to +3VSDGPU_MAIN for GC6-2.0



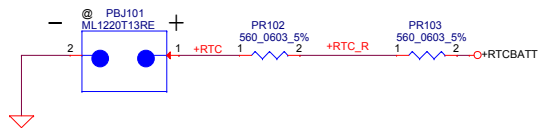
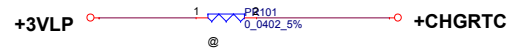
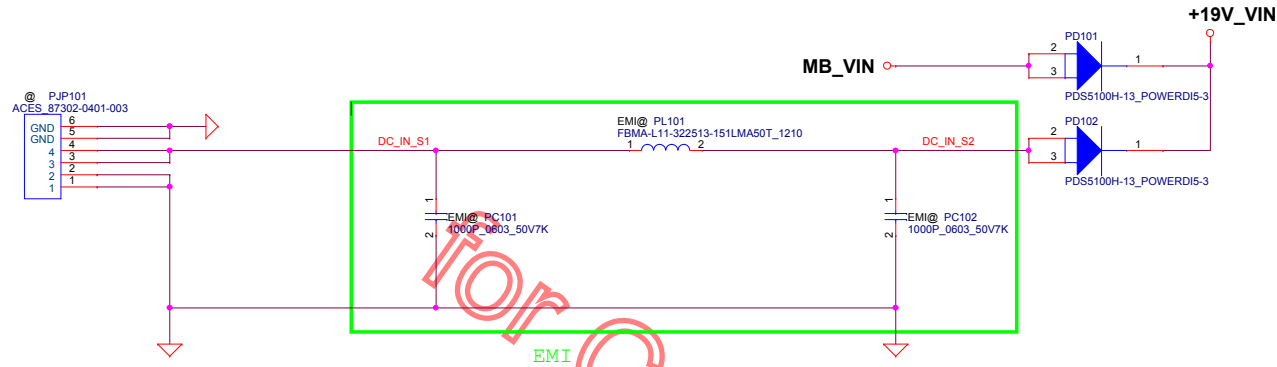
3VSDGPU_MAIN_EN From GPU

+3VALW to +3VM for Intel AMT
20mil(68mA)

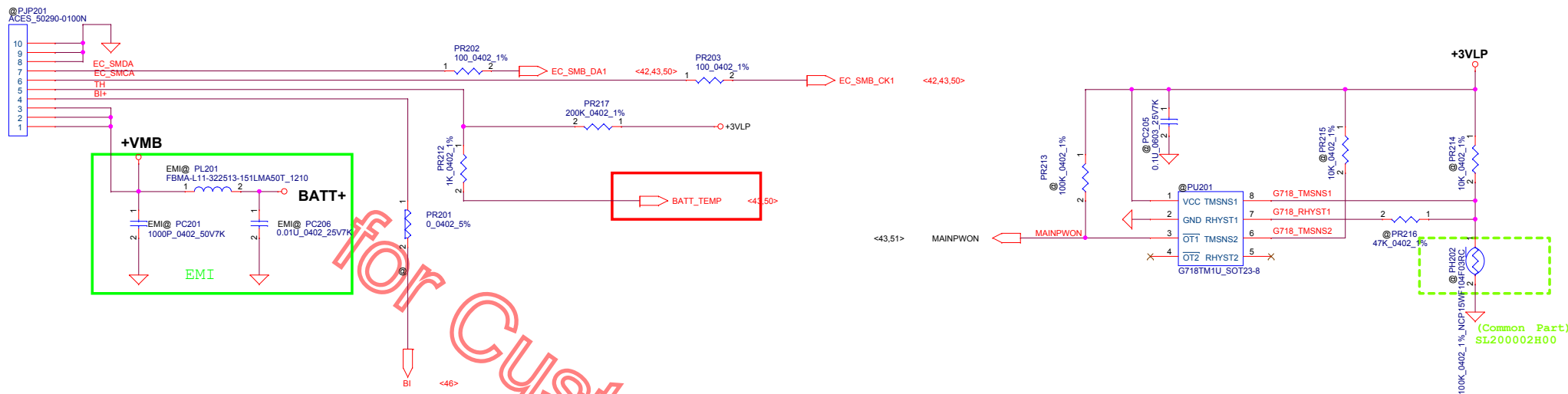


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				LA-D301P			0.2
				Date:	Friday, December 18, 2015	Sheet	47 of 63

2015/7/8
PD101 and PD102 SCS00002F00 change to SCS00002M00



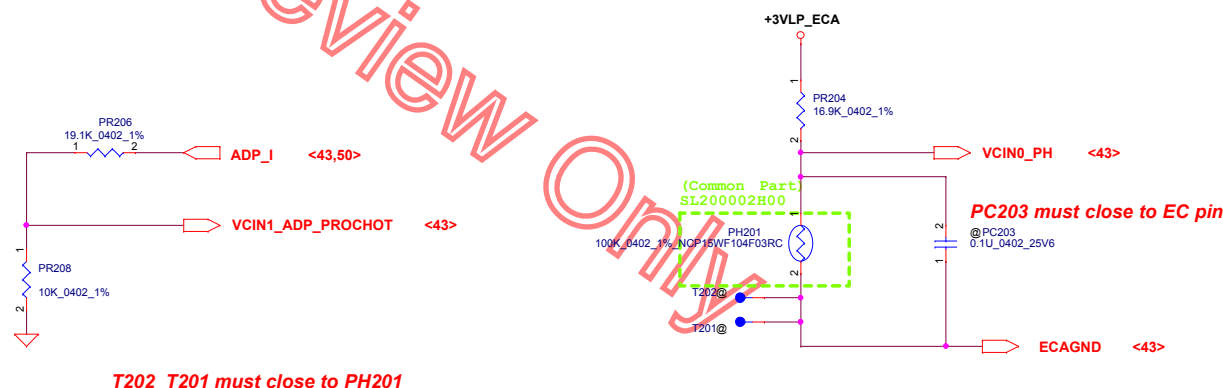
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				Custom	0.1
				B4DBU M/B LA-D301P	
				Date:	Thursday, December 17, 2015
				Sheet	48 of 63

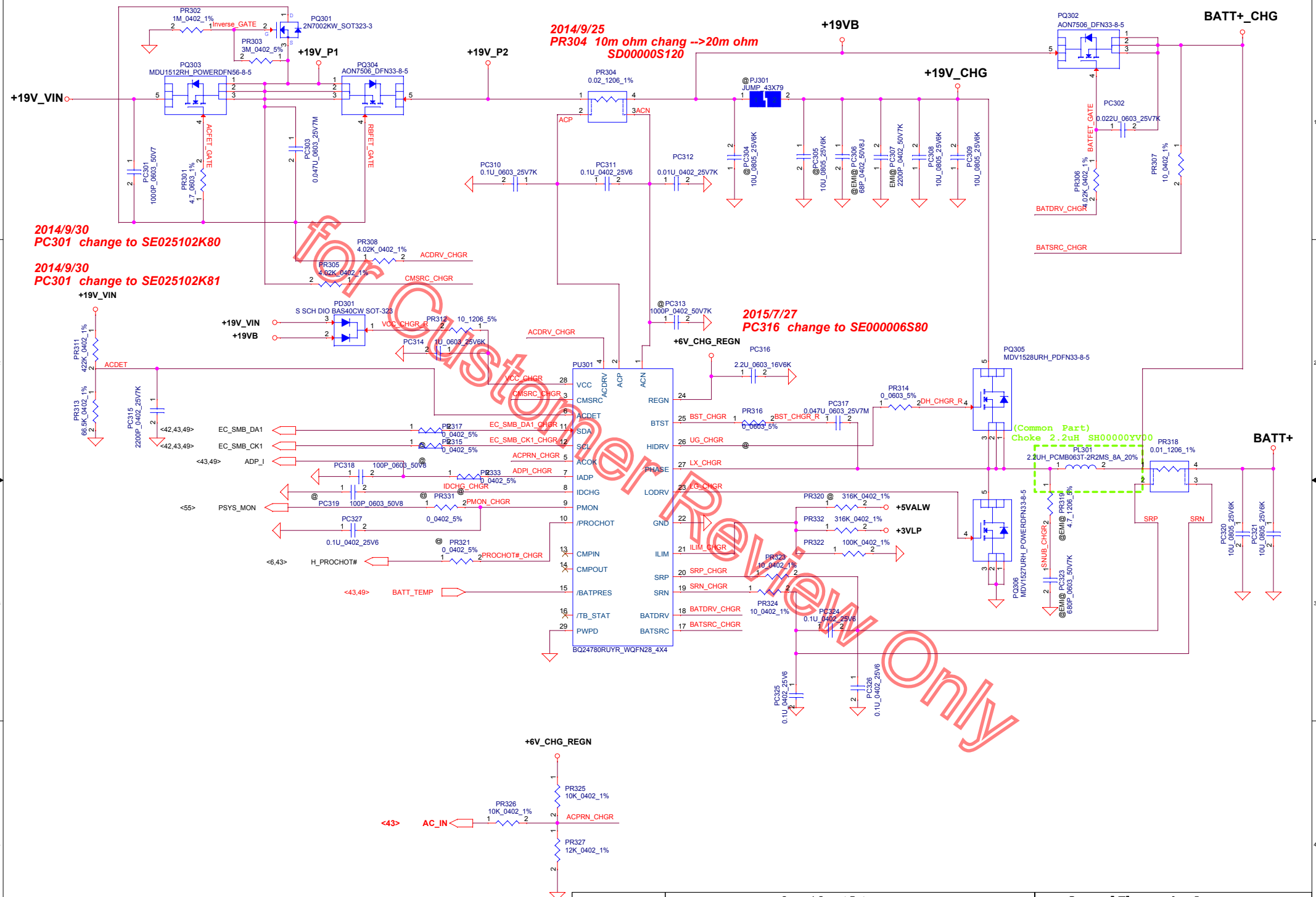


PH1 under CPU bottom side :
CPU thermal protection at 92 +3 degree C
Recovery at 56 +3 degree C

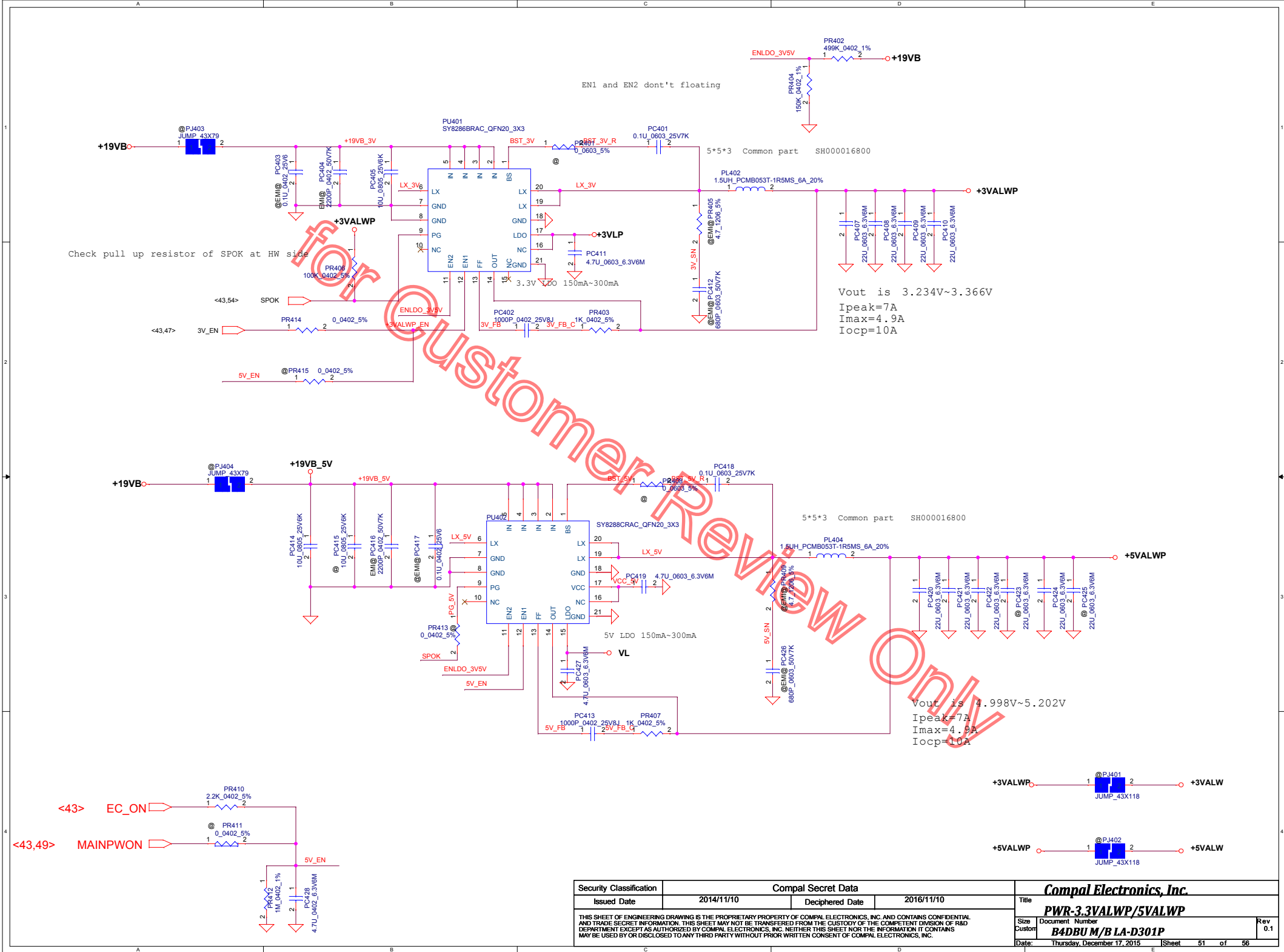
2015/07/09 update

For KB9022 sense 20mΩ	Active	Recovery
65W PR206 19.1K ohm SD034191280	84.5W, 0.61V	65W, 0.47V

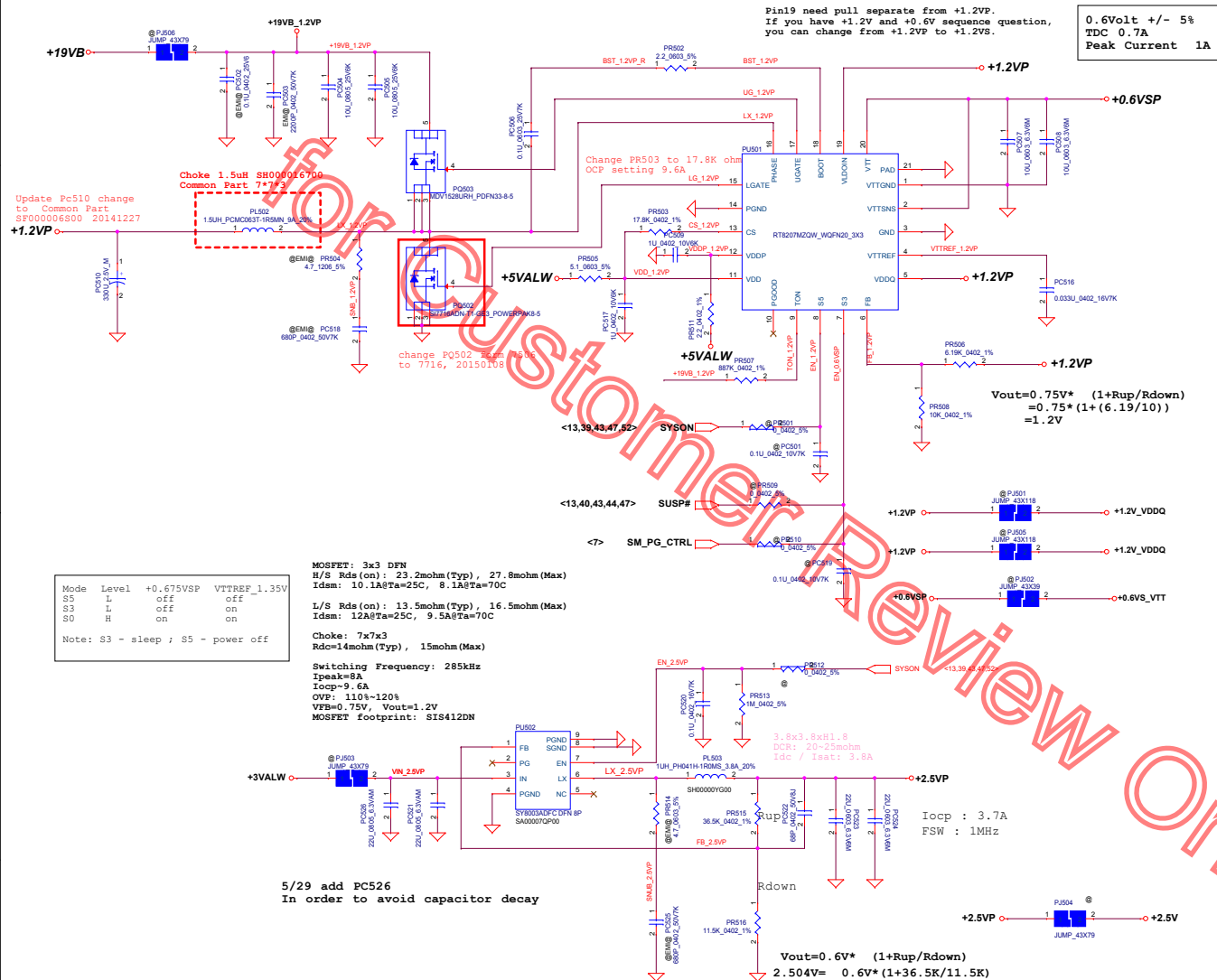


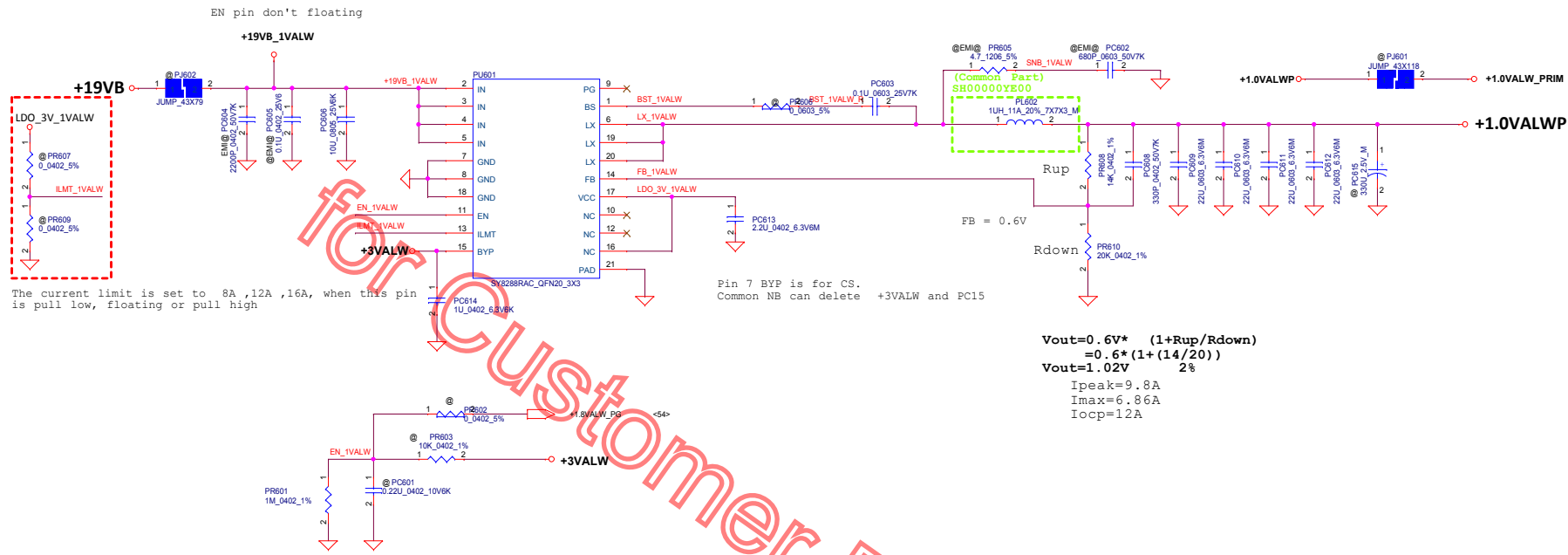


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Title		BQ24780					
Size		Document Number					
Custom		B4DBU M/B LA-D301P					
Date:		Thursday, December 17, 2015		Sheet		50 of 56	



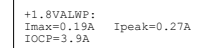
Module model information
RT8207M_V1.mdd For Single layer
RT8207M_V2.mdd For Dual layer





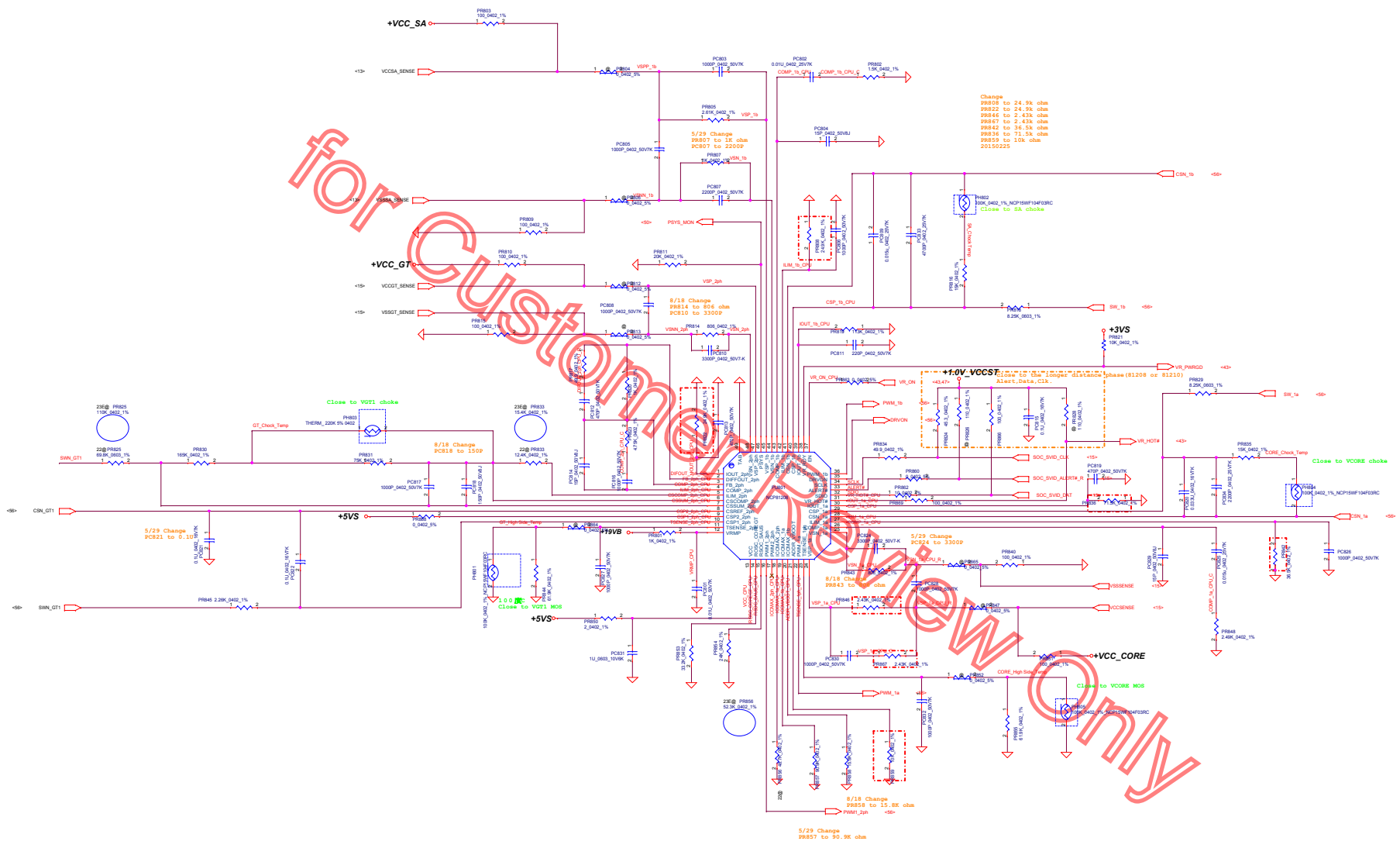
Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2014/11/10	Deciphered Date	2016/11/10	Title	+1.0VALWP
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					B4DBU M/B LA-D301P
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				Rev	0.1

SY8032_V2.mdd

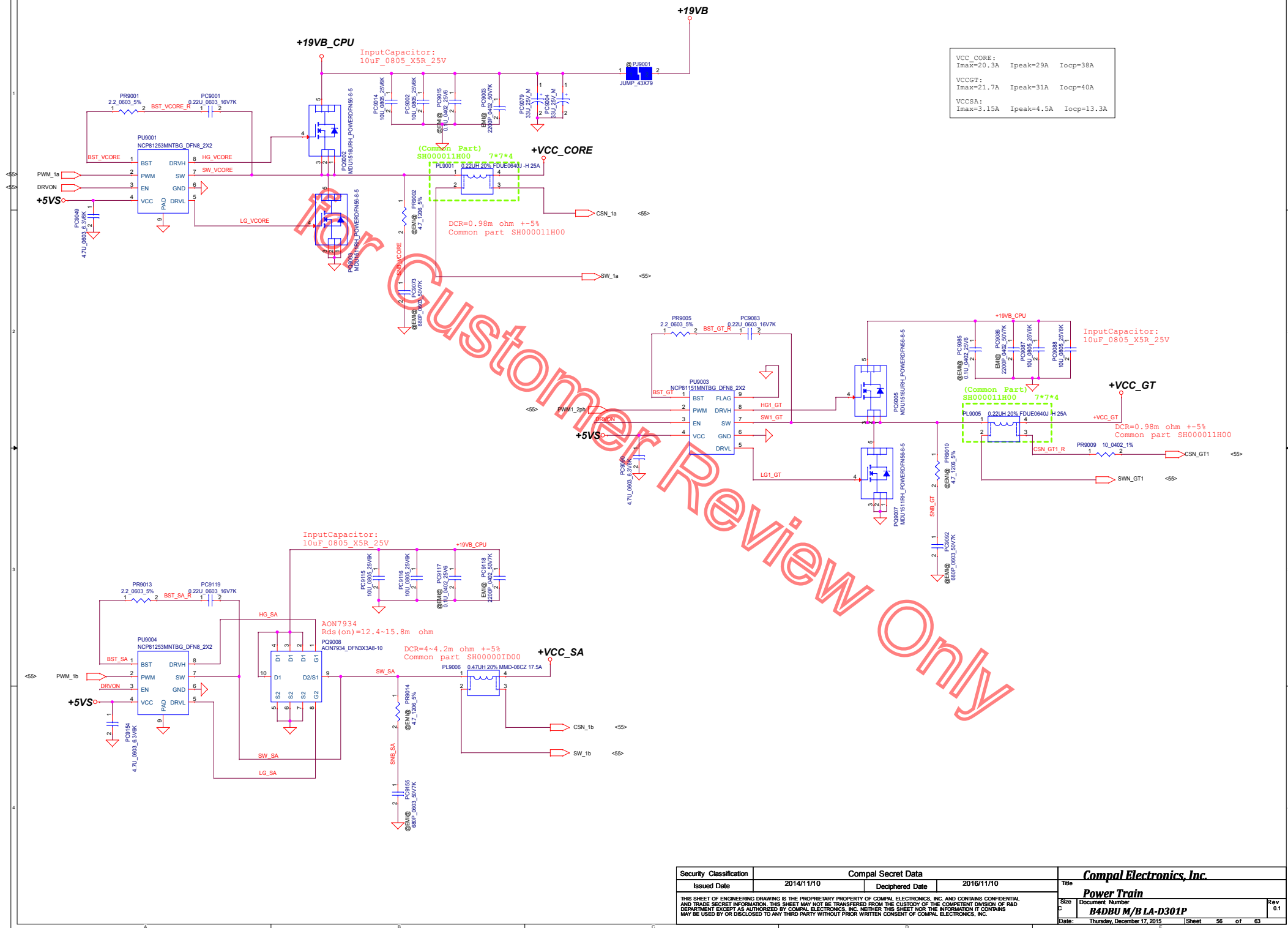

$$V_{out} = 0.6V * (1 + R_{up}/R_{down})$$

$$V_{out} = 0.6V * (1 + (20/10)) = 1.8V$$

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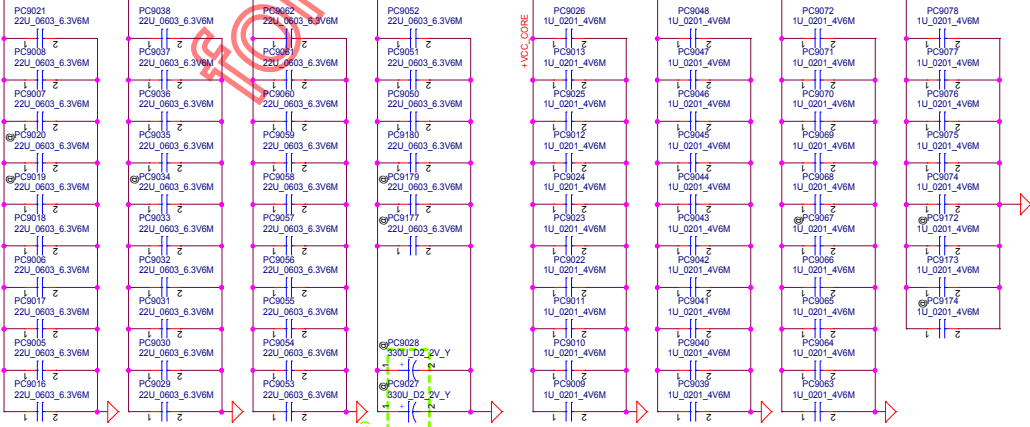
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Rev	1	Issued Date	2014/11/10	Rev	1
84DBU M/B LA-D301P		Drawing Number		Sheet 50 of 51	



Total VCORE Output Capacitor:

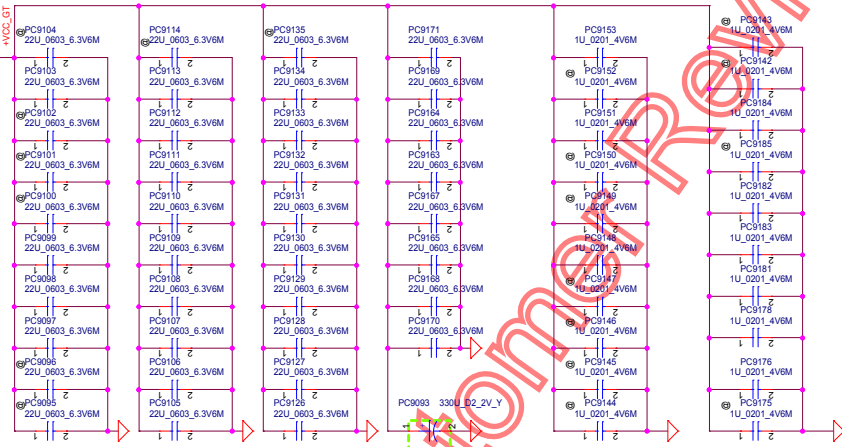
2015/07/09
22uF_0603_28PCS
1uF_0201_35PCS
UNPOP: 0603_3PCS, 0201_3PCS, 330uF_R9_2PCS

+VCC_CORE



2015/07/09
DZ*1 22uF_0603*30 1uF_0201*9
UNPOP: 22uF_0603*8 1uF_0201*11

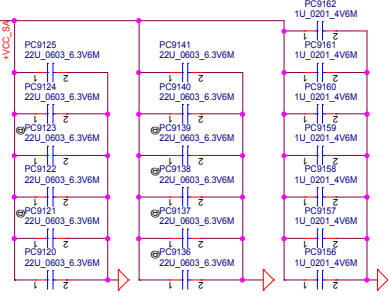
+VCC_GT



1u_0201 SE0000000200856
22u_0603 1 SE00000000000

2014/07/03
22uF_0603*6 1uF_0201*7
UNPOP: 22uF_0603*6

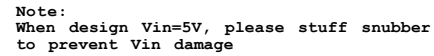
+VCC_SA



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Rev		Size		0.1	
Date		Sheet		57	63

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				A3	0.1
				Document Number B4DBU M/B LA-D301P	
Date:	Thursday, December 17, 2015		ISheet	58	of 63

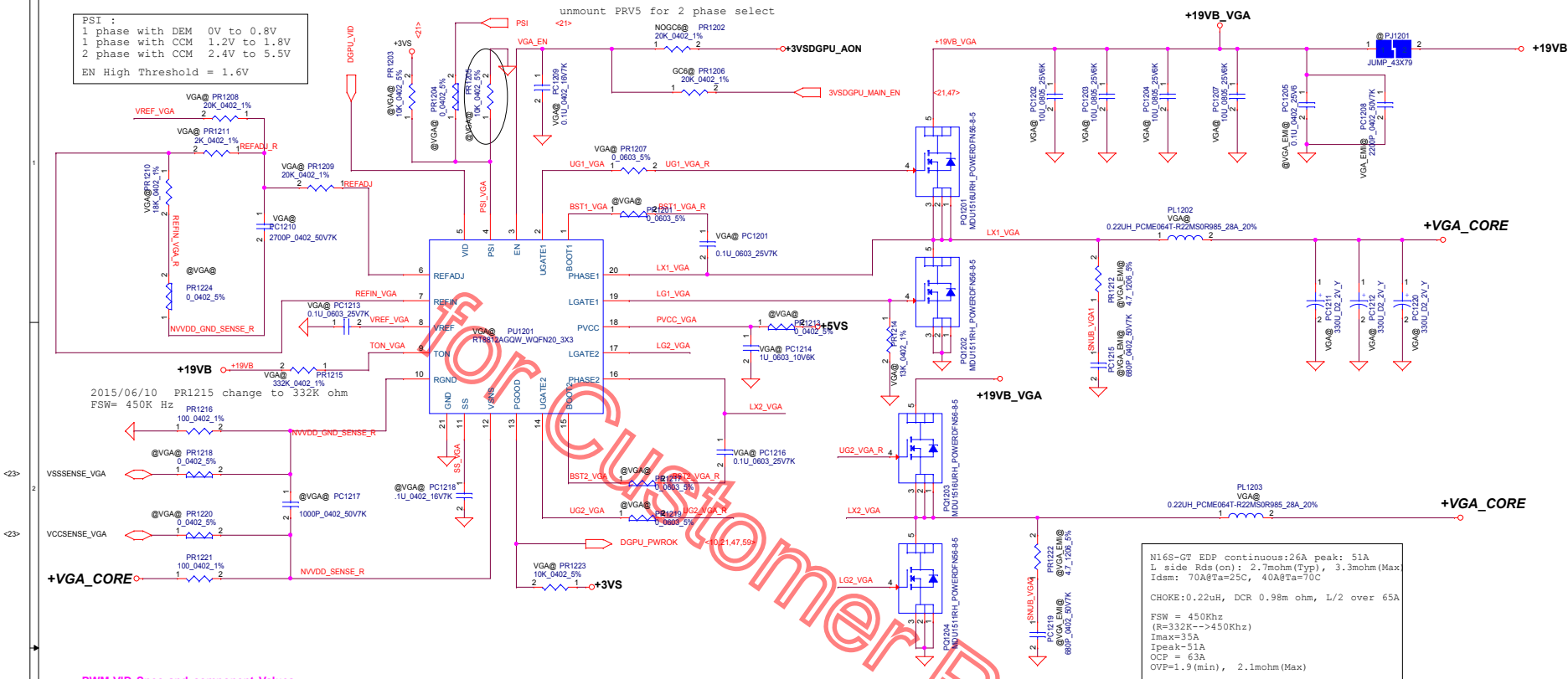
SY8032_V2.mdd



$$V_{out} = 0.6V * (1 + R_{up}/R_{down})$$
$$= 0.6V * (1 + (7.68/10)) = 1.061 \quad (1.01\%)$$
$$I_{max} = 0.77A, \quad I_{peak} = 1.1A, \quad I_{ocp} = 3.5A$$

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Date				Thursday, December 17, 2015	Sheet 59 of 63

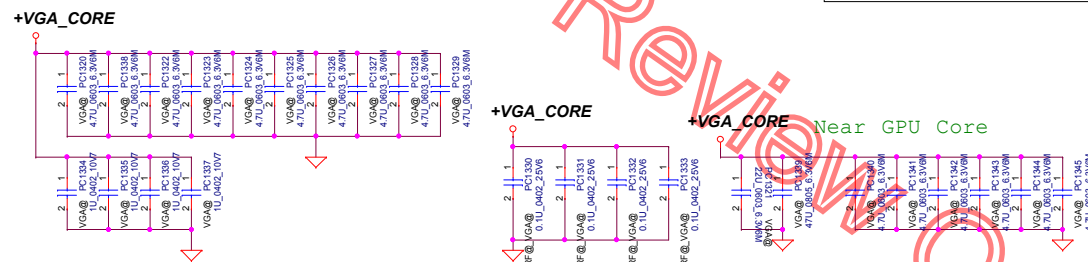
PSI :	
1 phase with DEM	0V to 0.8V
1 phase with CCM	1.2V to 1.8V
2 phase with CCM	2.4V to 5.5V
EN High Threshold	= 1.6V

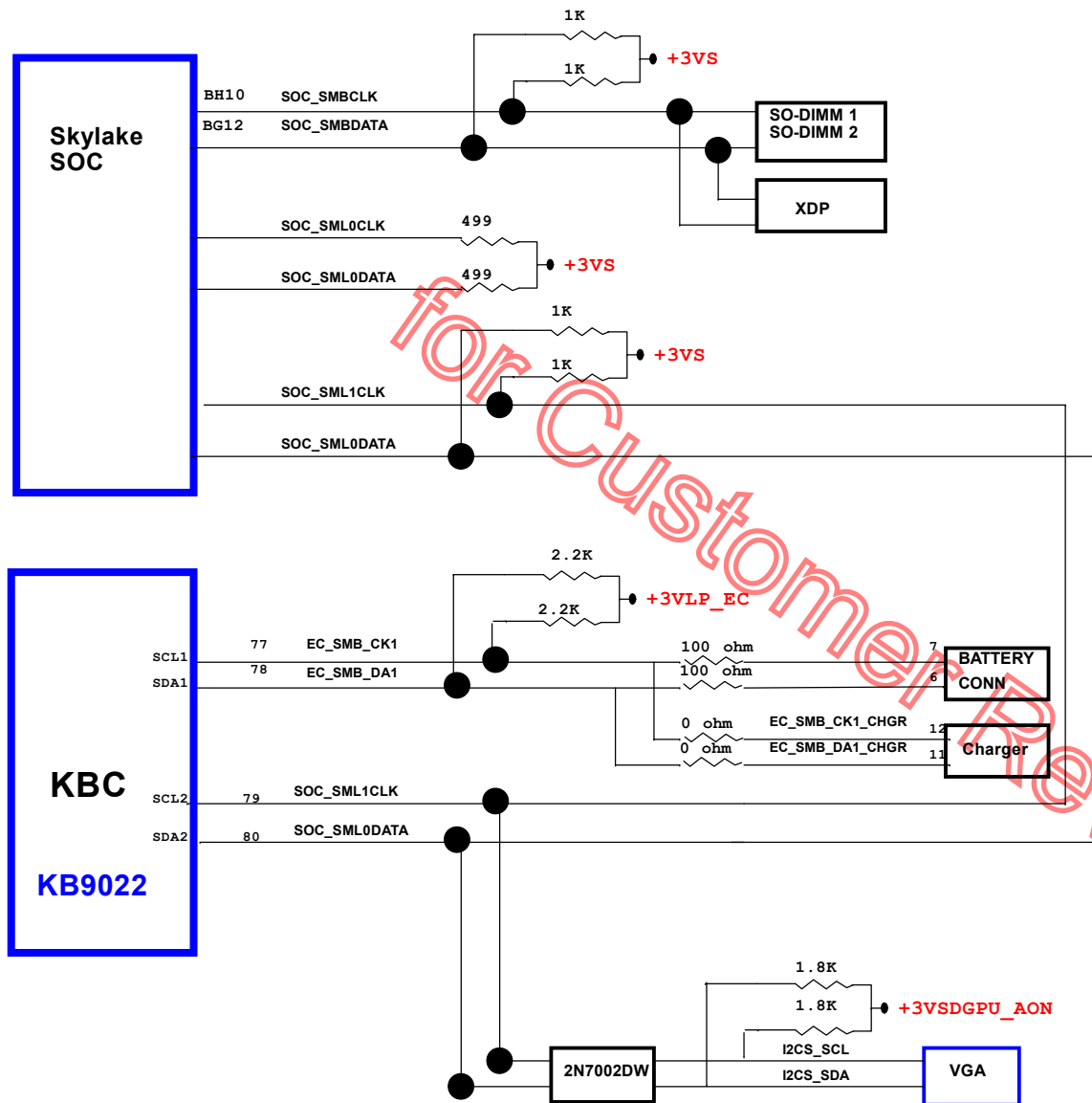


PWM-VID Spec and component Values

PWM-VID Spec		Config B	Config C	Config D
Vmin		0.6V	0.65V	0.9V
Vmax		1.2V	1.15V	1.15V
Vboot		0.9V	0.9V	1.028V
Voltage step		6.25mV	25mV	12.5mV
N of Voltage level		96	20	27
Rrefadj	PR	20K	39K	20K
Rref1	PR	20K	30K	7.5K
Rboot	PR	2K	3K	0
Rref2-PR1209 +PR1212	PR	18K	24K	6.2K
	PR	0	3K	1.74K
C	PC	2.7nf	1.8nf	5.6nf

N16S-GT
N16V-GM





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					SMBUS Routing Table
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				B4DBU M/B LA-D301P	0.1
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Version change list (P.I.R. List)

Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	Date	Phase
01	Design Change.	X1 Code : SE158225K80	02	50	PC316 change to SE000006S80	8/25	DVT
02	Design Change.	ON FAE suggest to modify Parts	02	55 57	PR814 and PR843 change to 806 ohm. PR858 change to 15.8K ohm. PC810 change 3300P. PC818 change to 150P. Add PC 9008, PC9031, and PC9007.	8/25	DVT
03							
04							
05	Design Change.	For Type-C function	03	51	PU402 change to SA00008YM00	10/7	PVT
06	Design Change.	Change 0 ohm to short pad.	03		PR1001, PR101, PR1103, PR1201, PR1204, PR1213, PR1217, PR1219, PR1224, PR201, PR315, PR316, PR317, PR333, PR401, PR408, PR501, PR510, PR512, PR602, PR606, PR705, PR804, PR806, PR812, PR813, PR847, PR852, PR864, PR865 change to short pad	10/22	PVT
07							
08							
09							
10							
11							
12							
13							
14							
14							

for Customer Review Only

EVT->DVT

0810

- 1. Remove RPC8
- 2. Change the BOM structure of CD36 and CD34 to @
- 3. Change UL3's part number to SA000028Y10
- 4. Change U67's part number to SA000071O10
- 5. Add U5004's part number SA00008E710
- 6. Change U5007's BOM structure to TBT@
- 7. Change U1's part number to SA00007UJ10
- 8. Remove U61, C818
- 9. Change BOM structure of RC62 and RC63 to POP
- 10. Connect RC18.2 to Codec PIN 31 (for MIC function)
- 11. Remove RC240
- 12. Add C5227
- 13. Add R5251, R5252
- 14. Change D44's part number to SC300003S00
- 15. change BOM structure PC@ to @

0812

- 1. JLIID1. 4 Connecto to +3VLP
- 2. change type C connector's part number to LTCX006Z3BL
- 3. remove D16

0813

- 1. change type C connector JUSB2's footprint from lotes_ausb0139-p001a_24 to JAE_DX07S024XJ1_24P-T

0817

- 1.change back TYPE C connector to SP011504212
- 2.change D29 and D30's part number to SC300003S00, same as D44
- 3.remove R630,R631,R633,R665,R667,R668,R669,R671
- 4.C5126,C5121,C5118,C5117 change to @ for HDMI
- 5.C5201,C5202,C5197,C5196 change to 0201 for TBT
- 6.Add C5239 0.1u on +3VS (JFP1) for EMI
- 7.C480,C633 change to RF@ for RF
- 8.ADD C5237 68P on +3VS(JTP1) for RF
- 9.ADD C5238 68P on +3VS(JFP1) for RF
- 10.ADD C5232 68P on +3VS(JDMIC) for RF
- 11.ADD C5229, C5230, C5231 0.1u+2200p+68p on +19VB for RF
- 12.ADD C5235, C5236 68P*2 on +3VS(JKB) FOR RF
- 13.ADD C5228, R5253 00HM+22P (RPC9) FOR RF
- 14.ADD C5233 0.1u on +5VALW(JIO1) for EMI
- 15.ADD C5240 68P on +5VALW(JIO1) for RF
- 16.ADD C5241 @RF@ for RF
- 17.Change C5241's connection to ESPI_CLK_R
- 18. Change R5173's connection to EC_TBTA_RESET

0818

- 1. Change C5227 to @
- 2. Change C633 to @
- 3. Change C5179~C5182 package to 0201
- 4. Modify the connection of U26.9(G_INT2)

0819

- 1. Change package of R630, R631, R633, R665, R667, R668, R669, R671 to short pad
- 2. Add C5242, C5243, C5244, C5245 for EMI
- 3. Change package of U5005 to SOP8
- 4. R1579-->@, R1581-->POP

DVT->PVT

1008

- 1. C5244, C5243, C5242, C5245 change to EMI@
- 2. D17, D18, D19, D20, D21, D34, D23, D24 Change to SC40000AT00
- 3. R443, R444, R445 change to vpro@
- 4. R4903 change to 15K for DVT Board ID
- 5. R1579-->@, R1581-->POP
- 6. R5203-->@, R5173-->POP
- 7. UL3, U60 Change to SA000079400
- 8. SW1-->@
- 9. CL14 change to 0603
- 10. JREAD1 PIN10's connection from +3VALW to +5VALW
- 11. CD41, CD42, CD43 change to 0402
- 12 add 16M BIOS ROM on UC2

1012

- 1. Connect DET_SIG#_R to UCPU1 pin AY5

1015

- 1. Change below items to short pad :
RC238,RC245,RC55,RC56,RC12,RC130,RC131,
RC168,RC186,RC188,RC208,RC140,RC143,RC141,
RC192,RC175,RC148,RC173,RC154,RC198,RC209,
RC149,RC176,RC156,RC197,RC161,RC163,RC172,
RC167,RC187,RC162,RC171,RC169,RC164,RC190,
RC152,RD45,RD47,RD46,R550,R549,R23,R5248,
R664,RC229,RC19,RC20,R486,R487,R873,R441,
R442,R661,R5193,R1580,R5210,R5209,R5192,
R5194,R5197,R5198,R4953,R514,R645,
2. Change U5007's part number to SA00008C310

1016

- 1. Update power schematic 1016

1016a

- 1. Add R5254, R5255 for Draco_SL reserve

1018

- 1.Change R23, R5248, RC130, RC131, R486, R487 back to 0ohm resistor

1027

- 1. Change U67's part number to SA000071O00
- 2. SUSCLK R5252 POP->@
- 3. R5250 TBT@->@TBT@
- 4. Add LAN Chip UL1 R3 Part Number SA000081G50
- 5. Replace SP050006F00 to SP050006B10

PVT->PreMP

1209

- 1. Change R1581 to @
- 2. Change R1579 to TBT@
- 3. Change U60 to @
- 4. Change UC3's to 3VM
- 5. BOARD ID Change to PreMP Value
- 6. Add RC248, RC249

1216

- 1. R525 changes to 10K
- 2. C5232 changes to 0.1U
- 3. PIN UC1.R40 connect to +3VALW PRIM with 2.2K resistor
- 4. add U5008 for 3VALW and 3VALWP

1217

- 1. U5009.4 Connect to 3VLAWP
- 2. Add Q2021, R5258, R5259 for Discharge
- 3. Q2021.3 Connect to SUSP#

1218

- 1. Add C5251 for EC_RSMRST#

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